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RESEARCH PAPER

A 24 GHz wideband monostatic FMCW radar system based on a single-channel SiGe bipolar transceiver chip

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In this paper a monostatic frequency-modulated continuous-wave (FMCW) radar system around a center frequency of 24 GHz with a wide tuning range of 8 GHz (≈33%) is presented. It is based on a fully integrated single-channel SiGe transceiver chip. The chip architecture consists of a fundamental VCO, a receive mixer, a divider chain, and coupling/matching networks. All circuits, except for the divider, are designed with the extensive use of on-chip monolithic integrated spiral inductors. The chip is fabricated in a SiGe bipolar production technology which offers an f_T of 170 GHz and f_{max} of 250 GHz. The phase noise at 1 MHz offset is better than −100 dBc/Hz over the full-tuning range of 8 GHz and a phase noise of better than −111 dBc/Hz is achieved at 27 GHz. The peak output power of the chip is −1 dBm while the receive mixer offers a 1 dBm input referred compression point to keep it from being saturated. The chip has a power consumption of 245 mW and uses an area of 1.51 mm². The FMCW radar system achieves a power consumption below 1.6 W. Owing to the high stability of the sensor, high accuracy mesaurements with a range error $< \pm 250$ μm were achieved. The standard deviation between repeated measurements of the same target is 0.6 μm and the spatial resolution is 28 mm.

Keywords: Radar Architecture and Systems, SI-based Devices and IC Technologies

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I. INTRODUCTION

Frequency-modulated continuous-wave (FMCW) radar systems offer potential for a variety of applications in the frequency band around 24 GHz. One important field is high precision industrial measurements, where good accuracy with range errors below 1 mm are mandatory. Other important applications are short range radars (SRR) for vehicular radar systems for a variety of tasks like blind spot detection or pre-crash sensors. For both fields of applications a cost-effective, robust, and simple design is imperative as most of the applications do not allow for expensive systems. Hence, an SiGe monolithic microwave integrated circuit (MMIC) design is favored over a III–V MMIC [1] or a discrete design [2].

The most important factor of a high quality FMCW radar system is proper design of microwave circuits, in this case the MMIC. The design of the MMIC strongly influences measurement errors in the whole radar system. key features in the design of an MMIC for an FMCW radar system are high dynamic range, good phase noise performance, and flat output power.

Another important factor for an FMCW radar system is bandwidth. The azimuth resolution can be improved by increasing carrier frequency, antenna size, or by the use of arrays. Range resolution on the other hand, which is defined as the minimum distance for two targets in close proximity which can still be separated from each other, is limited by ramp bandwidth of the FMCW radar system. Recent advances in published radar systems are showing bandwidths of 4 [3], 10 [4], and 25.6 GHz [5] in the W-band and even more at higher frequencies. The radar in this paper offers a bandwidth of 8 GHz, which results in very high relative bandwidth of 33%, in the K-band, where the assembly of the radar system is much easier to handle and very cost effective. In this frequency region, it is also possible to build cost effective phased array systems with sufficient output powers for airborne radar imaging (e.g. small unmanned aerial vehicles at low altitudes), neglecting today's existing frequency regulations.

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II. SYSTEM CONCEPT

The block diagram of the proposed radar system is given in Fig. 1. High frequency parts of the radar system are integrated in a low-power SiGe MMIC. For robust operation all on-chip circuits and interfaces are realized fully differential. The 24 GHz

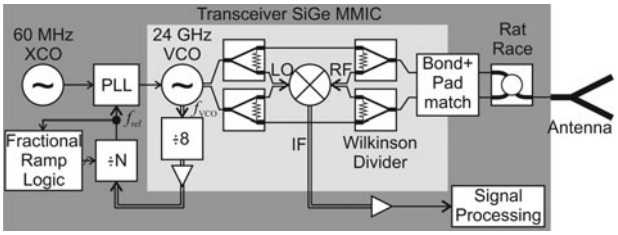

Fig. 1. Block diagram of the presented transceiver chip in an FMCW radar system. The 24 GHz VCO is stabilized by a fractional-N PLL. Differential signal paths are drawn with double lines.

signal is generated by a fundamental voltage-controlled oscillator (VCO) which is then divided by two Wilkinson dividers to generate the local oscillator (LO) and transmit signal. Antenna duplexing is also performed on-chip with two additional Wilkinson dividers to achieve a monostatic configuration similar to [5]. Thus, only one K-band interface with pad and bond wire compensation network has to be integrated. The differential output is then combined with a rat-race coupler on a ceramic substrate and fed to the antenna via a K-connector. For stabilization in a phase-locked loop (PLL), a divide-by-8 circuit is also integrated on the MMIC. This reduces the complexity of the PLL control signal below 4 GHz, which enables the use of a commercially available PLL chip. This is then used to realize a single-loop PLL for highly linear fractional-N ramp generation of the radar system.

III. CHIP DESIGN AND EXPERIMENTAL RESULTS

In Section III(A) the design of various inductors will be discussed in detail alongside the design of the Wilkinson dividers. All circuits are designed for a single supply voltage of 5 V. The 24 GHz VCO and the divide-by-8 circuit will be presented in Section III(B) and Section III(C), respectively. The used 24 GHz receive mixer will be described in Section III(D) and in Section III(E) the transceiver chip will be shortly summarized.

A) Inductor design

The design of various monolithically integrated spiral inductors was one of the complex challenges in the development of this chip. Even though the circuit design with spiral inductors is more complex than the use of a design based solely on transmission lines, it offers some benefits at lower frequencies (<30 GHz). These are quality factors above 15, which are needed for, e.g., resonant inductance of the VCO, and compact lumped element structures compared to area consuming transmission line-based elements. Altogether the chip uses 20 spiral inductors, nine of them different, designed for their needs regarding quality factor and inductance. A design and optimization flow for spiral inductors, which was also used here, was presented in [6].

The compact lumped element Wilkinson divider in Fig. 2(a), including a bounding box, which is used for all inductors, uses only an area of 140 × 260 μm². A transmission line-based realization would need to use two transmission lines ($\lambda/4 \approx 1666$ μm) instead of the two spiral inductors shown in Fig. 2(a), which would result in a very large structure with high losses. Figure 2(b) shows the simulated S-parameter results of the Wilkinson divider. The loss of the Wilkinson divider is below 0.5 dB in the whole frequency range of interest (20.6–28.6 GHz) in addition to the ideal insertion loss of 3 dB. The matching at all ports and the decoupling between them is better than −16 dB in the same frequency range.

Furthermore, a bond wire and pad compensation network similar to the one in [5] is integrated on-chip to keep the reflections at the bond wires as low as possible.

B) 24 GHz Oscillator

The designed 24 GHz VCO is based on [7] and [6]. The schematic of the fully differential colpitts VCO is shown in Fig. 3(a). In order to achieve good phase noise performance the main inductances are here realized with high Q inductors (e.g. $Q_{L_B} = 30$) instead of microstrip lines.

The demands on the VCO for transceiver chip design are low phase noise, a high tuning range, and moderate output power at moderate power consumption. A high tuning range is achieved with the help of a two varactor design presented in [7]. With C_{in} being the capacitance into the transistor T_1 and L_B being the inductance at the base node of T_1 the oscillation frequency can be calculated as:

$$f_{\mathrm{OSC}} = \frac{1}{2\pi\sqrt{L_B C_{in}}}. \quad (1)$$

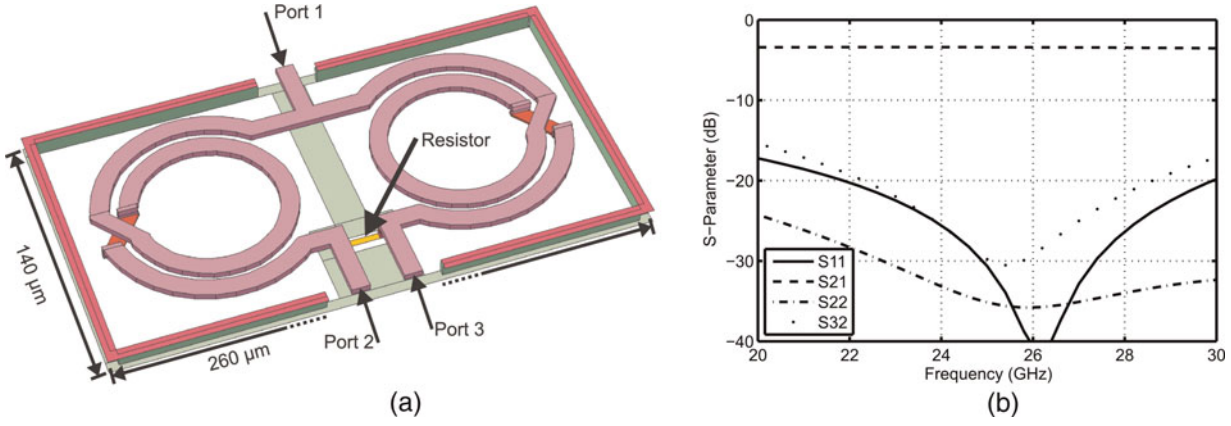

Fig. 2. (a) Realization of the compact Wilkinson divider with spiral inductors. (b) Simulated S-parameters (due to symmetry only 4 of the 9 curves are shown).

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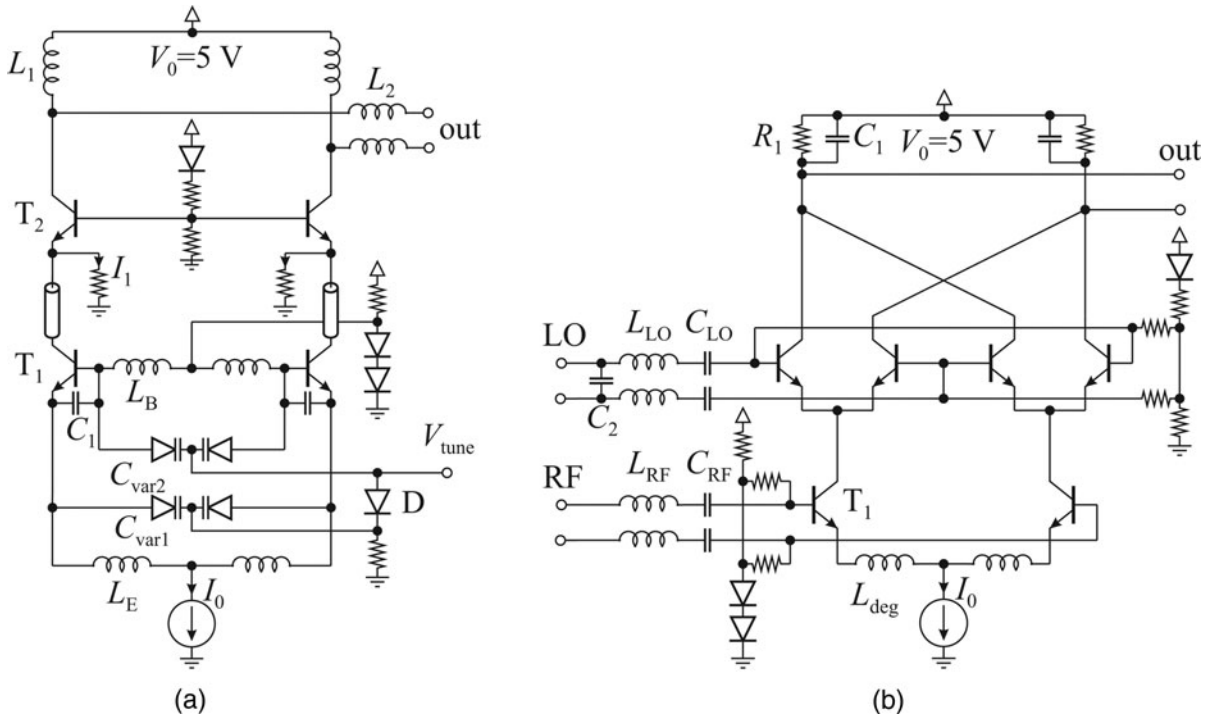

Fig. 3. (a) Schematic of the 24 GHz VCO. (b) Schematic of the 24 GHz receive mixer.

The second varactor C_{var2} increases the variation of C_{in} by ≈40% compared to a single varactor design. C_{var1} and C_{var2} are tuned via V_{tune} with nearly the same DC voltage drop across the two varactors with the help of the diode D.

To cope with the demand on moderate output power (>3 dBm), which is needed in order to drive the integrated mixer and achieve a high dynamic range, the transistor T_2 is biased with an additional current $I_1 = 2.5$ mA. However, to operate T_2 and T_1 at nearly the same f_T, the transistor T_2 is chosen to be 1.5 times bigger than T_1. In order to achieve good phase noise performance the transistors T_1 and T_2 are biased far below the current density for maximum f_T. Another point is an output network that is designed to deliver maximum output power into a 50 Ω system over the whole frequency range. This output network is realized with low Q inductors (L_1, L_2) instead of the high Q main inductances (L_B, L_E) of the VCO, as these inductors have nearly no impact on the phase noise. All of this take into account the current consumption for the VCO is 18.5 mA (92.5 mW) distributed into 10 mA for the core current I_o, 5 mA for the additional current of the cascode stage and 3.5 mA for the biasing networks.

In Fig. 4(a), the measured output power of the 24 GHz transceiver chip is plotted versus the oscillation frequency. An impressive tuning range of 8 GHz (33%) is achieved at room temperature. The plots agree well with the simulation

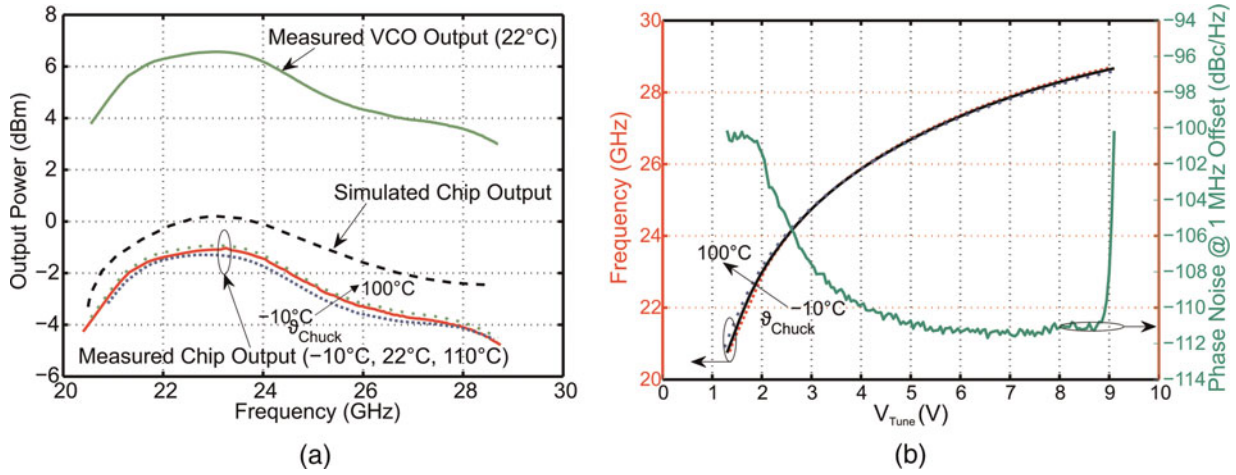

Fig. 4. (a) Measured output power versus frequency for three different chuck temperatures (−10°C, room (≈22°C), 100°C) in comparison to the simulation. The measured VCO output is the room temperature curve with the simulated losses (≈7.5dB@24 GHz) from the VCO output to the pads de-embedded. (b) Measured tune curve over temperature and phase noise versus tuning voltage.

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results. The difference in output power could be accounted for in neglected losses in either the measurement setup or the simulations. The maximum peak output power of the VCO is 6.5 dBm and the output power of the transceiver chip is −1 dBm. The flatness of the transceiver output power over the whole tuning range is better than 3.5 dB, which is quite good considering the ultra wide tuning range.

Figure 4(b) shows the measured tuning curve and the measured phase noise of the transceiver chip versus tuning voltage. At an offset of 1 MHz the phase noise is better than −111 dBc/Hz at 27 GHz. The phase noise at the lower end gets degenerated due to the pn-varactors getting operated nearer to the forward region or even operated slightly in the forward region. At the upper end the phase noise gets degenerated due to an avalanche breakdown of the used pn-varactors. However, even though it gets degenerated at the ends of the tuning range, the phase noise is still better than −100 dBc/Hz over the whole tuning range of 8 GHz.

The temperature dependence of the chip is excellent and is also shown in Fig. 4. The effect of a temperature change of 110°C on output power of the chip is negligible, shown in Fig. 4(a). The tuning characteristic of the transceiver is nearly unaffected by a temperature change of 110°C, this is shown with the three tuning curves for −10°C, room temperature (≈22°C), and 100°C which are lying nearly on top of each other. The tuning range is degenerated only by 300 MHz at the lower end for high temperatures. The phase noise is also only slightly affected by temperature (not shown).

The nearly temperature insensitive behavior of the VCO is achieved with three measures. The first measure is to operate the oscillating transistors of the VCO far below their maximum f_T not only to increase their noise performance. This measure helps to keep the transistors far off the steep f_T drop off in the high current region, because this f_T drop off has a strong temperature dependence which would otherwise degenerate the transistors performance.

For the second and third measure the schematic of the biasing networks for the oscillating transistors is shown in more detail in Fig. 5(a) simplified to the DC case. The second measure is employed through a dedicated transistor current source with resistive emitter degeneration to get a nearly temperature independent core current I_o. This luxury of a dedicated transistor current source is possible through the quite high system voltage of 5 V. The last measure is realized through the compensation of the temperature dependent U_{BE} voltages of the oscillating transistors. For that the current densities of the used diodes, which actually are the same type of transistors used in every circuit with a short collector and base, are exactly the same as for the oscillating transistors. With this the temperature dependent U_{BE_1} is nearly fully compensated with the also temperature dependent U_{D_1} and the temperature dependent $U_{BE_{3,4}}$ is compensated with U_{D_3}. With these two measures the oscillating transistors are kept in the exact same operating point over a wide temperature range. The same method is also employed in the biasing networks for the input stage of the receive mixer.

C) Static divide-by-8 circuit

The static 3-stage divider is based on master-slave D-type flip-flops realized in differential emitter coupled technique without additional emitter followers, which are commonly used in static frequency dividers for the highest frequencies. In Fig. 5(b), the schematic of one latch of the divider stage is shown, one divide-by-2 stage is made of two latches where the output of the second is negatively fed back to the input of the first latch.

The block diagram of the used divide-by-8 circuit, which is based on the static divider used in [6], is shown in Fig. 6(a). In addition, an output buffer is implemented to drive a load of 50 Ω, where the power consumption can be further reduced in the case of high impedance loads.

All transistors of the divider are of the same size but the transistors for the first stage are biased at a higher current density as they are operating at the highest frequency with a maximum system frequency of 28 GHz. The transistors are slightly bigger than the smallest allowed size in the technology, this is done a little bit conservatively to get a better tolerance on the transistors. The maximum current through one of the transistors of the first two latches is ≈0.75 times the current for maximum f_T, while the emitter coupled pair is biased at ≈0.375 times the optimum current density.

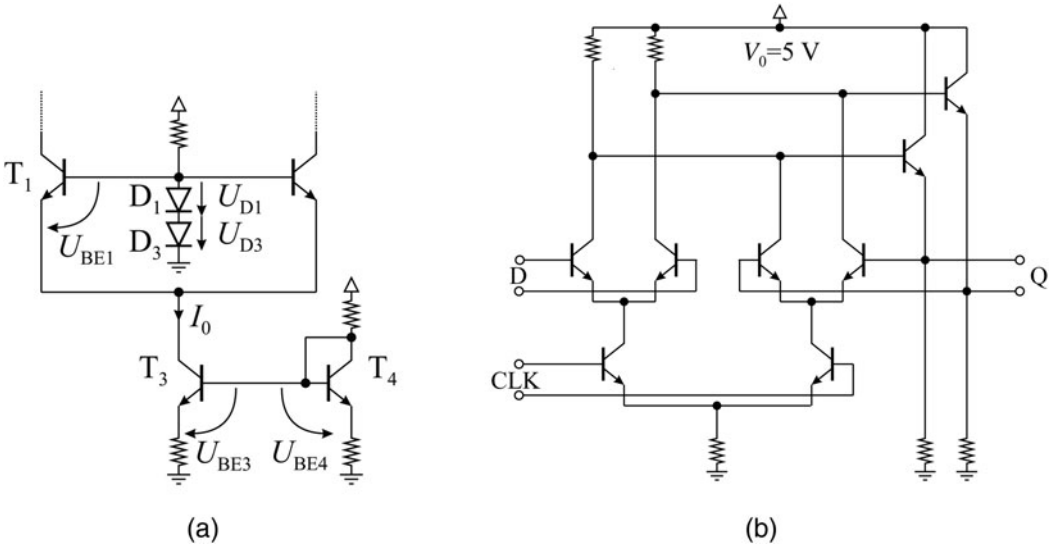

Fig. 5. (a) Detailed biasing network of the main oscillator transistors. (b) Circuit diagram from one out of six ECL latches of the static divider.

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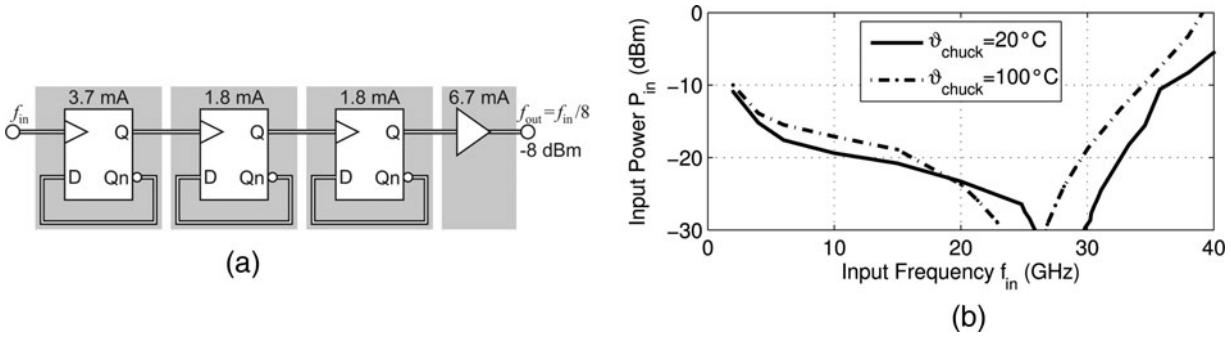

Fig. 6. (a) Block diagram of the static 3-stage divider with output buffer. (b) Measured input sensitivity of the divider for two different temperatures.

The measured input sensitivity of the divider is shown in Fig. 6(b). The measurement shows a good sensitivity for the frequency range between 20 GHz and 30 GHz, where an input power of less than −20 dBm is needed to drive the divider even at high temperatures of 100°C. The total current consumption for the divider is 14 mA (70 mW) consisting of 7.3 mA for the three divider stages and 6.7 mA for the buffer.

D) 24 GHz Receive mixer

In Fig. 3(b), the circuit topology of the 24 GHz receive mixer is shown. It uses a fully differential Gilbert-Cell topology. In order to achieve a high dynamic range of the mixer, good noise figure and high linearity are mandatory. To cope with these demands, the mixer uses the linearity increasing technique described in [8] based on inductive degeneration. The receive mixer also uses spiral inductors with different needs to achieve good overall performance and lower area consumption.

In order to achieve good noise figure and moderate conversion gain the mixer was designed for an LO drive power of −3 dBm to 6 dBm, which is easily supplied by the VCO discussed in Sectiion III(B). Here also bigger transistors with lower f_T are used for better noise performance. The total current consumption of the mixer is 16.3 mA (81.5 mW).

To achieve a wideband input and noise matching the demands on the used inductors were different. L_{LO} had essentially no need regarding the quality factor, hence rectangular design with small line width which can clearly be seen in Fig. 8(a). The design of L_{RF} and L_{deg} proved more challenging. To achieve an input match of better than −10 dB and good noise figure over the whole 8 GHz bandwidth a high Q inductor for L_{RF} is mandatory. Furthermore, a high Q inductor for L_{deg} was achieved due to the chosen compact differential design compared to L_{RF} and L_{LO}.

In addition to the increased linearity, inductive degeneration is used to achieve good input matching as well. Simplified input impedance into one symmetrical transistor can be expressed as

$$Z_{in}(\omega) = r_B + \frac{g_m \cdot L_{deg}}{C_{BE}} + j\omega\left(L_{deg} + L_{RF}\right) - \frac{j}{\omega \cdot C_{BE}}, \quad (2)$$

where r_B is the base resistance, C_{BE} is the base-emitter-capacitance of the input transistor T_1 of the mixer, L_{deg} is one part of the center-tapped spiral inductor and L_{RF} is the input spiral inductor. To keep the calculations simple only C_{BE} and r_B were considered, whereas especially C_{BC} and r_E have been neglected. The expression for input impedance has a frequency dependent imaginary part and a frequency independent real part with two effective degrees of freedom L_{deg} and L_{RF} which can be used for input matching. With proper choice of L_{deg} the frequency independent part can be tuned to 50 Ω to achieve a perfect match at the center frequency.

The measured conversion gain of the mixer versus frequency and simulated noise figure is shown in Fig. 7(a). The

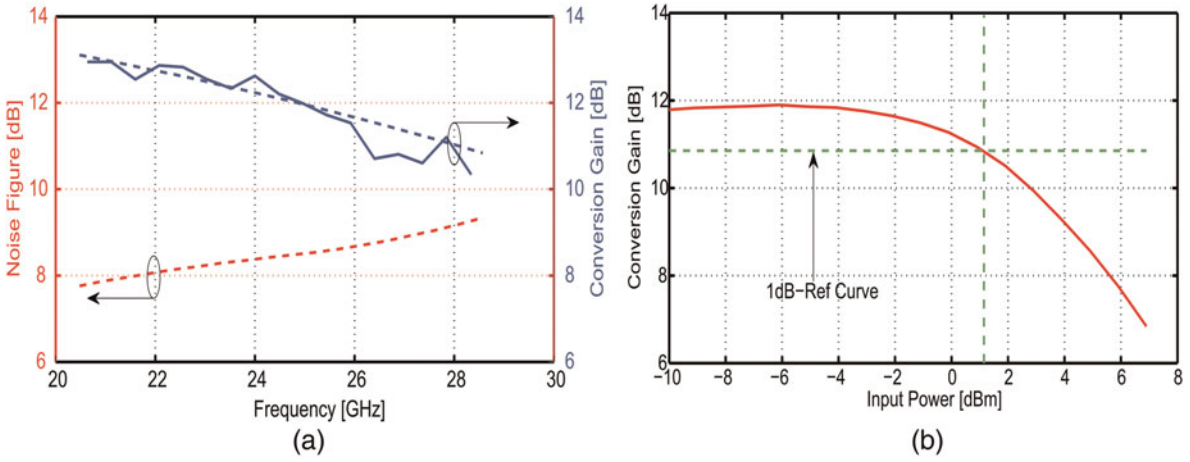

Fig. 7. (a) Measured conversion gain of the 24 GHz receive mixer in comparison to the simulation plotted over the oscillation frequency. Simulated result for the noise figure is also shown. (b) Measured conversion gain plotted versus RF input power with 1-dB reference curve to show input referred compression point.

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conversion gain at 24 GHz is ≈12.5 dB. In the intended frequency range of 8 GHz the flatness of the conversion gain is below 3 dB, which furthermore proves sufficient output power of the VCO over the whole frequency range. The difference to the simulated result is negligible. The noise figure in the 8 GHz band is better than 9.4 dB (only simulated result is shown), at 24 GHz it is ≈8.4 dB.

In Fig. 7(b), the measured result for the input referred compression point is shown. A compression point of ≈1 dBm is achieved with the chosen mixer architecture. This is high enough to cope with even a total reflection at the transceiver chips input–output pads.

Table 1. Summary of radar transceiver chip data.

Output power	−1 dBm
Output power drop between −10°C and 110°C	<0.5 dB
Tuning range	8 GHz
Phase Noise @1 MHz offset	<−100 dBc/Hz
Mixer input compression point (P_{1dB})	1 dBm
Mixer conversion gain	>10 dB
Mixer noise figure	<9.4 dB
Frequency divide ratio	/8
Supply current (5 V)	49 mA
Chip size	1628 × 928 µm²

E) 24 GHz Transceiver chip

In Fig. 8(a) the photograph of the SiGe transceiver chip is shown. The chip was fabricated in Infineon's 0.35 µm bipolar production technology B7HF200, which offers maximum transistor cut-off frequencies f_T of 170 GHz and f_{max} of 250 GHz at optimum current density. The total power consumption of the chip is 49 mA from a 5 V supply (245 mW). Table 1 summarizes the performance data of the transceiver chip. Owing to the used Wilkinson dividers an additional 3 dB has to be added to the noise figure and compression point and has to be subtracted from the conversion gain of the mixer for the transceiver chip.

IV. RADAR SYSTEM RESULTS

With the help of the presented 24 GHz transceiver chip a prototype radar system based on the system concept shown in Fig. 1 was developed. The developed board of the radar is shown in Fig. 8(b). It is fully powered from a USB interface with a power consumption below 1.6 W, where no further effort for optimization has been done for the prototype. Communication with a PC, where signal processing is performed, is also realized via the same USB interface. It is realized on a two-layered ceramic high frequency substrate (Rogers RO4003C) with the dimensions of 120 × 60 mm² mounted on an aluminum block for stability. For all parts, except for the SiGe transceiver chip, commercially available components are used, e.g. PLL chip, ADC, and DC–DC converters. For the PLL, an active loop filter and a PLL-Chip (Hittite HMC701LP6CE), which includes a fractional-N sweeper logic for linear ramp generation, are used.

The PLL was designed by carefully considering the K_{VCO} variation. This is quite a feat considering high K_{VCO} variation over the full tuning range of the VCO. Compare to Fig. 4(b) with a $K_{VCO} \approx 3.5$ GHz/V and a $K_{VCO} \approx 0.36$ GHz/V for the first and last volt of the tuning voltage, respectively. The loop bandwidth and the phase margin are set to ensure the best performance in the middle of the frequency band and to only slightly degrade the PLL performance at the edges of the used band.

To allow the usage of complete bandwidth of $B = 8$ GHz (20–28 GHz) in radar measurements a self-designed WR34 waveguide transition with a 20 dB standard gain horn antenna is used. Compared to [9] where an antenna was fed by a circular waveguide with a lower cut-off frequency of 23 GHz, this now enables the radar for measurements with additional 3 GHz bandwidth. The ramp time for the fractional-N synthesized FMCW ramp was set to $T = 4$ ms for all measurements, but faster ramps are also possible. The IF signal is further amplified and filtered with a low-pass corner frequency of $f_{IF,Max} = 400$ kHz after the down-conversion mixer and digitized with a 16 Bit 1 MSPS ADC. The maximum non-ambiguous range R_{Max} of the system in this setup is defined as:

$$R_{Max} = \frac{1}{2} \cdot c_0 \cdot f_{IF,\mathrm{Max}} \cdot \frac{T}{B} \approx 30 \text{ m}. \quad (3)$$

The PLL stabilization over the wide bandwidth without using offset PLL concepts (cf. [5]) or loop gain variation compensation techniques is quite challenging. Locking the PLL

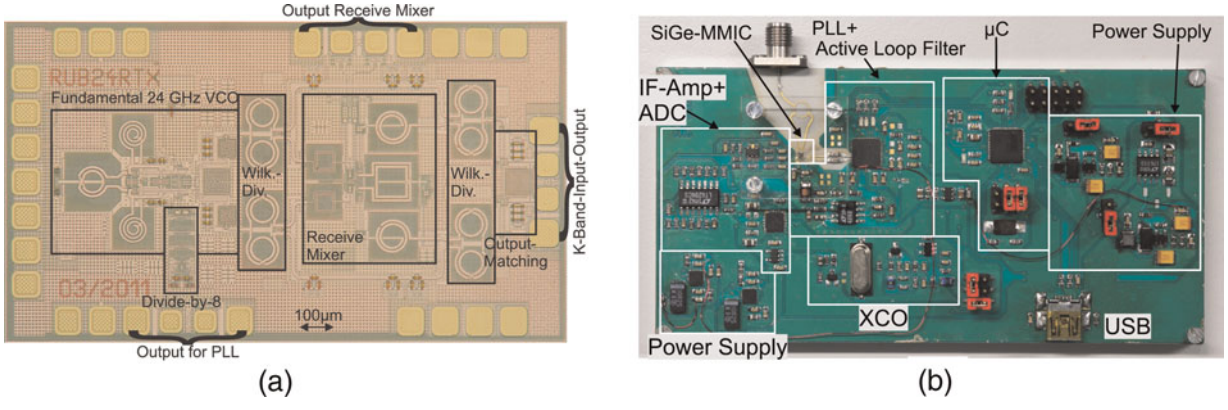

Fig. 8. (a) Photograph of the 24 GHz transceiver chip. The extensive use of monolithic integrated spiral inductors can clearly be seen. The overall chip size is 1.51 mm² including the pads. (b) Photograph of the complete system board with only a K-connector and USB connection needed for full operation.

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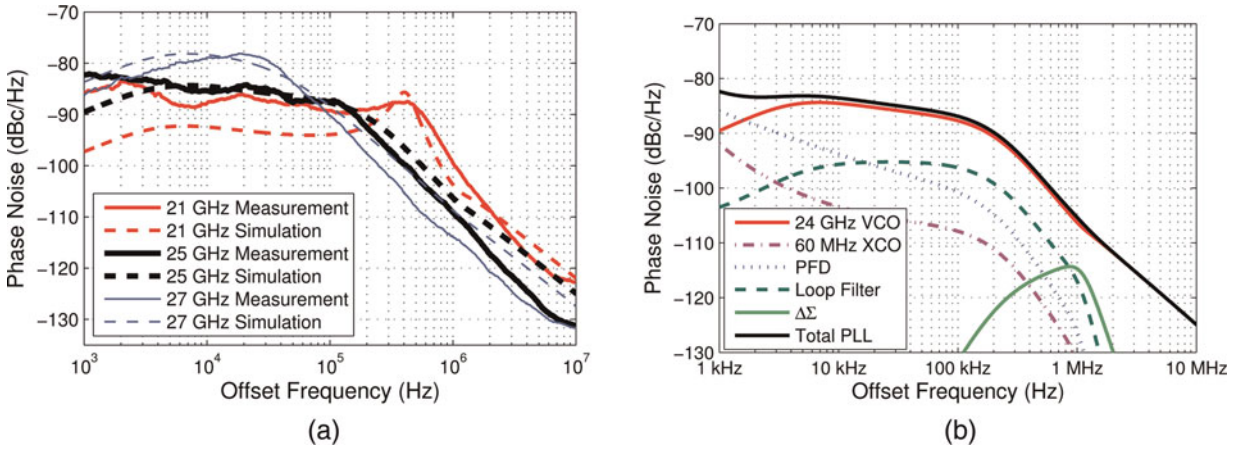

Fig. 9. (a) Measured phase noise of the PLL-stabilized radar system at different frequencies (fractional mode) in comparison to the simulation. The phase noise was measured using a spectrum analyzer at the 2.92 mm K-connector of the system board. (b) Phase noise contribution of significant PLL parts.

over the complete bandwidth of 8 GHz was achieved by a carefully designed loop filter, which offers a good trade-off between PLL stability and integrated phase noise for the used band. The VCO gain (K_{VCO}) is changing from 3.5 GHz/V (20 GHz) to 360 MHz/V (28 GHz). With the used loop filter at 25 GHz center frequency, a loop bandwidth of 100 kHz and a phase margin of 68 deg is achieved. For the lower frequencies (21 GHz) the loop bandwidth changes to 340 kHz (27 deg phase margin) and for higher frequencies (27 GHz) it decreases to 48 kHz (78 deg phase margin). For the loop filter design and simulations the "PLL analysis and design tool" from Hittite microwave was used, which offers great flexibility for varying VCO gains, etc.

In Fig. 9(a), the phase noise of the PLL-stabilized radar system in fractional mode at a lower (21 GHz), a middle (25 GHz), and a higher (27 GHz) frequency of the covered bandwidth are shown in comparison with the simulation. Some small discrete spurs which are caused by the on-board USB-interface are not shown, they are expected to be gone with a more optimized board layout. The differences to the simulations are small. Only for the lower frequency of 21 GHz the phase noise at offset frequencies $<$200 kHz is slightly degraded. Owing to the very small phase margin of 27 deg some peaking can also be seen at the loop bandwidth of 340 kHz. Owing to the fact that for most measurements a Hanning or similar window function is used and the PLL is still stable in the performed measurements this slightly degraded performance at the band edges is acceptable.

Over the complete bandwidth in fractional mode an in-loop phase noise of ≈ -78 dBc/Hz is achieved. At the center frequency the phase noise performance is even better with (≈ -82 dBc/Hz). Figure 9(b) shows a phase noise contribution plot to clarify the sources of phase noise, which contributes to the overall phase noise performance.

To prove ramp linearity and stability of the radar system, Fig. 10(a) shows a range plot of a single target scenario and a zoomed plot of the scenario within Figure 10(b). In close distances the reflections of the used horn antenna can be seen and a strong target at ≈ 5.6 m can be seen. The sidelobes can be further reduced by using window functions. Here a rectangular window (correction factor of 1.21 for -6 dB width) is used in signal processing to show the resolution, which can be achieved with the 8 GHz bandwidth resulting in the theoretical value of:

$$\delta_{range,-6\ dB,rect} = \frac{c_0}{2\Delta f} 1.21 = 22.67\ \text{mm}. \tag{4}$$

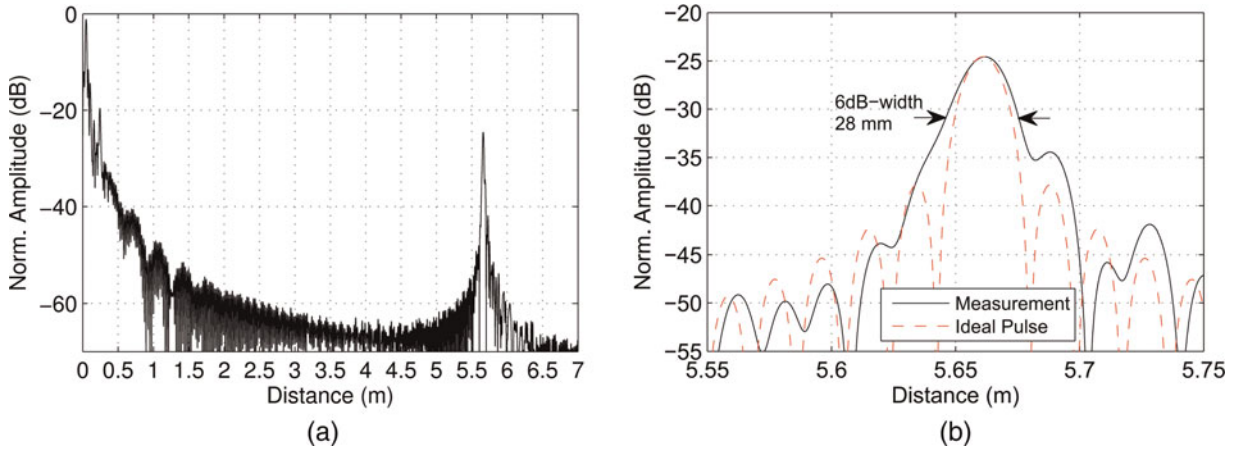

Fig. 10. Spectrum of a measured IF signal for a single target in the range up to 6 m (a) and a detailed view of the target (b). No window function or amplitude correction is applied. The achieved resolution is 28 mm for a real target scenario.

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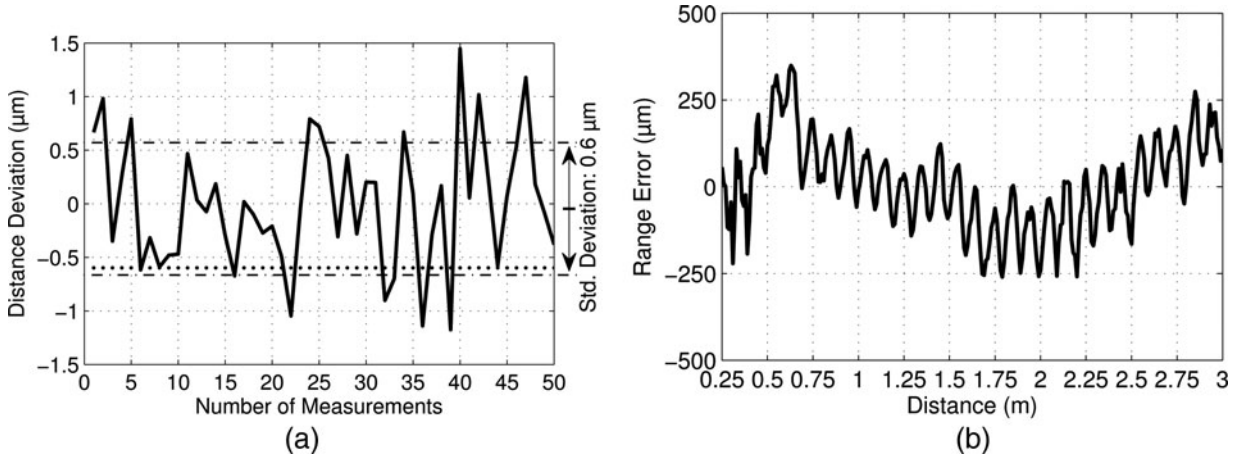

Fig. 11. (a) Deviation of multiple distance measurements. A simple pulse center algorithm was used for signal processing. (b) Measured range error of the 24 GHz FMCW radar system compared to the linear positioning unit.

Although the measured −6 dB width of 28 mm for the real target scenario (metal plate) does not perfectly match the theoretical value, an ideal target scenario with a short coaxial 2.92 mm K-cable delivers a perfect fit to the theoretical value for this bandwidth with 23 mm and the main lobe in this scenario has good agreement with an ideal si-pulse (not shown), which let us expect a sufficiently high ramp linearity. The mismatch in the real target scenario is due to dispersion in the self-designed, and mainly hand-crafted, horn antenna and waveguide, which was not compensated for in signal processing. There, it widens the width of the target. In addition, it is very sensitive regarding misalignment of the plain target.

To additionally show the stability of the sensor repeated accuracy measurements for a single-target at ≈ 0.71 m distance are done with 50 consecutive measurements, which is shown in Fig. 11(a). The achieved standard deviation is better than 0.6 µm with a maximum deviation below 2.7 µm.

The range error of the radar system over 3 m range is shown in Fig. 11(b). A corner reflector was moved on a linear positioning unit from 0.25 cm to 3 m. The observed range error is ≈ ± 250 µm. The ripple is assumed to stem from inaccuracies of the linear actuator unit, which was used as reference. This has been cross-checked with an existing 80 GHz radar system which achieved a precision of better than 4 µm [10] delivering the same ripple as the presented 24 GHz radar system. For determining the position of the target a simple pulse center algorithm was used.

V. CONCLUSION

A complete wideband 24 GHz radar system based on a SiGe transceiver chip is presented. Quite impressive is the area consumption of 1.51 mm² due to the monolithic integrated planar spiral inductors. Another impressive key feature of the MMIC is the high bandwidth of 8 GHz (33%), which is to the best of the authors knowledge a record bandwidth around 24 GHz. The results are achieved with a power consumption of only 245 mW.

Furthermore, a complete FMCW radar system prototype is presented with a range error of ≈ ± 250 µm. The full tuning range of the transceiver chip was stabilized in a PLL resulting in a ramp bandwidth of 8 GHz with an in-loop phase noise better than −85 dBc/Hz over the ramp bandwidth. Moreover, the in-loop phase noise can be further decreased with an offset PLL similar to [2] and [5]. The precision could be further improved with a better measurement setup with a phase slope algorithm as used in [2] or the algorithm used in [10]. The results of the radar system are summarized in Table 2, where an additional loss of 1 dB due to the K-connector, bond wires, and the ceramic substrate is accounted for.

Table 2. Summary of FMCW radar system data.

Output power	−2	dBm
Tuning range	8	GHz
Phase noise in PLL	< −78	dBc/Hz
Range error	± 250	µm
Jitter Std. Dev.	< 0.6	µm
Spatial resolution/theor.	28/22.67	mm
Supply current (5 V, USB Powered)	320	mA
Radar system size (without antenna)	120 × 60	mm²

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