International Journal of Microwave and Wireless Technologies, 2013, 5(1), 65–70.
doi:10.1017/S1759078712000748

RESEARCH PAPER

Low-power CMOS LNA based on dual resistive-feedback structure with peaking inductor for wideband application

MENG-TING HSU, SHIH-YU HSU AND YU-HWA LIN

This paper presents a low-power and low-noise amplifier (LNA) with resistive-feedback configuration. The design consists of two resistive-feedback amplifiers. In order to reduce the chip area, a resistive-feedback inverter is adopted for input matching. The output stage adopts basic topology of an RC feedback for output matching, and adds two inductors for inductive peaking at the high band. The implemented LNA has a peak gain of 10.5 dB, the input reflection coefficient S_{11} is lower than −8 dB and the output reflection S_{22} is lower than −10.8 dB, and noise figure of 4.2–5.2 dB is between 1 and 10 GHz while consuming 12.65 mW from a 1.5 V supply. The chip area is only 0.69 mm² and the figure of merit is 6.64 including the area estimation. The circuit was fabricated in a TSMC 0.18 um CMOS process.

Keywords: Low-noise amplifier (LNA), Low power, Resistive feedback, Inverter

Received 7 February 2012; Revised 30 October 2012

I. INTRODUCTION

In recent years, the demand for high-speed and high data-rate wireless communication has been increasing gradually. Wideband and ultra-wideband (UWB) low-noise amplifiers (LNAs) have been an area of research interest for many years. In order to achieve high-speed data transmission, LNAs have to meet stringent requirements of gain, bandwidth (BW), noise, and dynamic range. The UWB system is a new wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low-power and high data rates. Although the UWB standard has not been completely defined, most of the proposed applications allow transmission of signals between 3.1 and 10.6 GHz.

Recently, several wideband amplifiers have been demonstrated for either UWB or optical communication applications. In [1, 2], the wideband performances are achieved by using multi-order matching networks; therefore, large chip sizes are unavoidable. Wideband and low-power amplifiers using feedback topologies are popular and have been recently reported in papers [3–8]. Some of these papers emphasized the low-power consumption for UWB application [3–6]. A modified low-power distributed amplifier with programmable-gain control is proposed in [7]. The differential topology of CMOS LNA for 3–5 GHz wideband application is addressed in [8].

National Yunlin University of Science and Technology Press, 123 University Road, Section 3, Douliou, Yunlin 64002, Taiwan, Republic of China. Phone: +886 5 534 2601 4322
Corresponding author:
M.-T. Hsu
Email: hsumt@yuntech.edu.tw

In this work, we propose a wideband low-power and LNA based on dual resistive-feedback topology. The first stage is the adopted inverter stage with inductive peaking technique for input matching. The second stage, an RC feedback buffer with peaking inductor load is coupled with resistive feedback to drive the 50 Ω output load. The circuit design is discussed in Section 2. We also discuss that the process of the choice with peaking inductor plays an important role on the circuit design. The measurements and simulation results of the low-power LNA are shown in Section 3. Finally, the conclusion is in Section 4.

II. CIRCUIT DESIGN

A) Resistive-feedback inverter for input matching

Figure 1(a) shows the conventional resistive-feedback inverter gain cell without inductive peaking. The BW of the conventional feedback inverter is dominated by the time constant at the input/output node [9]. Therefore, the operating BW will be limited by the parasitic capacitors of the CMOS transistors. Figure 1(b) shows the inverter cell with inductive peaking. The peaking inductor is used to extend the 3 dB BW of the inverter stage. However, since the peaking inductor is loaded at the gate terminals of the NMOS and PMOS of the inverter stage, the peaking inductor is loaded by the gate–source capacitors (C_{gsn} and C_{gsp}) from the gates of both the NMOS and PMOS. If we neglect the small feedback capacitor C_{gd} between the gate and drain terminals, the transfer function

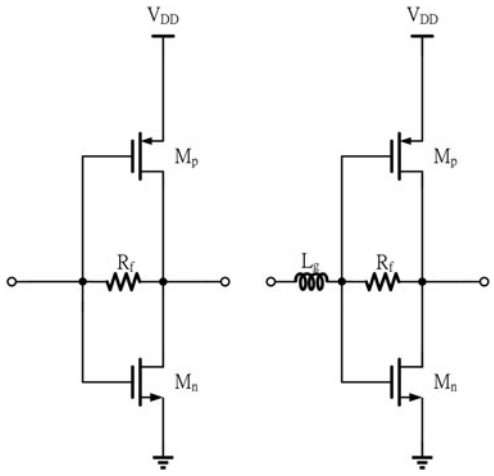

Fig. 1. Single stage of resistive-feedback inverter. (a) Conventional one without inductive peaking. (b) Inverter stage with inductive peaking technique.

of Fig. 1(b) can be derived as [9]:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + s^2 L_g(C_{gsn} + C_{gsp})} \times \frac{1 - R_f(g_{mp} + g_{mn})}{1 + R_f(sC_{dsn} + sC_{dsp} + r_{on}^{-1} + r_{op}^{-1})}, \quad (1)$$

where g_{mn} and g_{mp} are the transconductance of the NMOS and PMOS, respectively. The C_{dsn} and C_{dsp} are the capacitors between the drain and source terminals, and here r_{on} and r_{op} are the output resistance of the NMOS and PMOS, respectively.

From equation (1), resultant poles from the conventional inductive peaking inverter cell and the proposed inductive splitting-load peaking inverter cell are $(\sqrt{(L_g(C_{gsn} + C_{gsp})})^{-1}$. It can be observed that the location of the pole in the proposed structure is boosted to a higher frequency. To investigate the frequency responses of the circuit structures of Fig. 1, their simulated gain performances are plotted in Fig. 2. It is noted that the bias voltage and the device size are the same in the simulations. Compared with the conventional structures in Fig. 1(a), the proposed structure can effectively extend the 3 dB BW to a higher frequency without additional power consumption. It is noted that the peaking inductors in Fig. 1 are all EM-simulated rather than ideal inductors, in order to include all the parasitic effects.

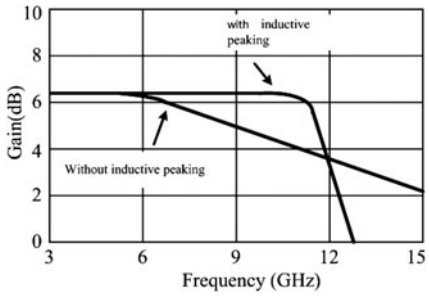

Fig. 2. Simulated gain performances of single-stage inverters according to Fig. 1.

B) Second-stage resistive-feedback amplifier

The basic idea for a circuit of a resistance-feedback wideband amplifier using peaking inductor L in the series with M_1 on the second input stage is shown in Fig. 3(a). The high-frequency simplified model depicted in Fig. 3(b) can be studied and analyzed, and R_g is the equivalent gate resistance. In the circuit, M_1, Z_L and Z_F are the transistor, load, and feedback impedance, respectively. According to Miller's theorem, we can determine that the equivalent input impedance is $Z_{f1} = Z_F/1 + |A_v|$, and the output impedance is $Z_{f2} = Z_F/1 + \left|\frac{1}{A_v}\right|$. We assume that the circuit is connected to a source generator whose impedance R_s is typically 50 Ω. In the first approximation, we can derive the analytic expressions of the input impedance (Z_{inf}), noise figure (NF), and gain ($|A_v|$) as the following equations [10]:

$$|A_v| \approx \left(\frac{1/sC_{gs}}{sL + 1/sC_{gs} + R_g}\right) g_m(Z_L||Z_{f2}) \approx \frac{g_m}{s^2 LC_{gs}}(Z_L||Z_{f2}), \quad (2)$$

$$Z_{inL} = sL + \frac{1}{sC_{gs}} + R_g, \quad (3)$$

$$Z_{inf} \approx \left(\frac{Z_F}{1 + |A_v|}\right) Z_{inL}, \quad (4)$$

$$NF \approx 1 + \frac{2}{3}\frac{1}{g_m R_S}\left(\frac{1}{R_S} + \frac{R_S}{Z_F^2}\right) + \left(\frac{f}{f_T}\right)^2 \frac{2}{3} g_m R_S + \frac{R_S}{Z_F}, \quad (5)$$

where f_T is the transition frequency of the MOSFET. The NF of the first stage is minor when compared to the second stage and it can be ignored by the way of balance circuit. The first reason is the function of the first stage of the circuit is adopted to extend 3 dB BW. The second is because of the input matching. The noise of low-frequency band is strictly depressed by the forward gain. Therefore, the contribution on noise is smaller than in the second-stage amplifier.

In order to achieve a trade-off between gain and input impedance matching, the device size can be tuned and determined properly in the design process. From equations (2) and (4), the inductor results in a slight decrease of the gain. If the inductance is properly chosen, it can affect the 3 dB BW extension. Owing to the input impedance of the transistor, it can be viewed as capacitive, and it will be the RC filter function to form the narrowband response. Therefore, if the peaking inductor is accurately chosen and inserted into the input node of the circuit, the frequency response of the BW can be expanded. This is the reason why we use the peaking inductor in the circuit. The leading phase of the inductor can be balanced with the lagging phase of the capacitor.

Dealing with NF and BW, it was found that high A_v and small Z_F lead to a wider −3 dB BW. However, due to the NF degradation, a smaller Z_F is not a desirable approach in equation (5). Therefore, high-voltage gain (A_v) or large transconductance gm (compatible with "term is magnified by

https://doi.org/10.1017/S1759078712000748 Published online by Cambridge University Press

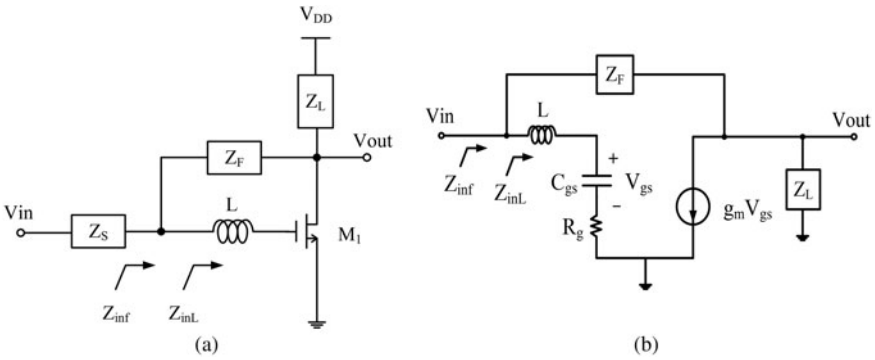

Fig. 3. (a) Proposed topology of a resistive feedback with peaking inductor *L*. (b) Simplified model of a resistive feedback with peaking inductor *L*.

gm") is a better choice to increase the BW and also lower the NF. Nevertheless, in CMOS technology, because of poor transconductance, higher A_v requires a dramatically larger and prohibitive DC current. All the internal noise sources of the amplifier can be represented by the input referred shunt noise current and series noise voltage sources in a two-port noise model. The detailed analysis can be referenced in [10]. However, the feedback resistance is usually pretty large so that the added noise to the amplifier is limited; moreover, the R_f term is magnified by $g_m{}^2$. The large value of R_f will also result in a little deviation of the G_{opt} of the amplifier from the value without feedback. This characteristic can be observed from Fig. 4. G_{opt} is the optimum conductance at the condition of the optimum value of source admittance for minimum NF.

The purpose of LNA input matching design is to enhance the gain and minimize the NF. However, the input matching conditions for maximal gain and minimal NFs are usually different. For CMOS amplifiers, the optimal noise input that matches admittances with and without shunt feedback will not vary much if $g_m{}^2 R_f$ is quite large. On the other hand, the shunt feedback provides a way to manipulate the amplifier input impedance. Figure 4(a) shows the maximal gain input matching reflection coefficient (Γ_{max}) and optimal noise input matching refection coefficient (Γ_{opt}) of the common-source amplifier without feedback from 1 to 10 GHz. After adding the shunt feedback, the Γ_{opt} of the amplifier is barely moved, and the Γ_{max} is shifted toward the Γ_{opt} as shown in Fig. 4(b). Hence, a better design trade-off between the gain and NF of the broad-band CMOS LNA can be obtained. In other words, there is larger deviation for both Γ_{opt} and Γ_{max} without a shunt feedback loop. If the shunt loop is added into the circuit, then the locus of Γ_{opt} and Γ_{max} can be achieved simultaneously.

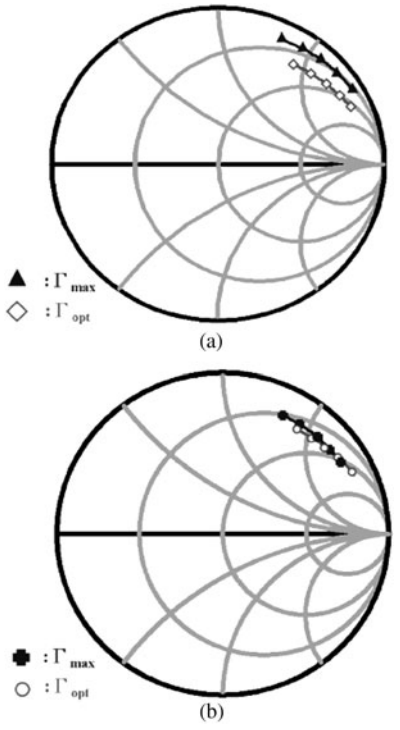

Fig. 4. Source impedances of the common-source CMOS amplifier for maximal gain (Γ_{max}) and optimal NF (Γ_{opt}) from 1 to 10 GHz: (a) without shunt feedback and (b) with shunt feedback.

C) The proposed topology

The proposed low-power and LNA is shown in Fig. 5, which consists of the input matching network that is implemented by a resistive-feedback inverter. The resistive-feedback inverter consists of M_p, M_n, and R_1; the output stage is the resistive-feedback amplifier, which consists of M_1, L_2, L_3, L_4, R_2, R_f, and C_f. Although, R_3 and L_4 can control the gain behavior at the low band, the gain control at the high band is determined by M_1 and feedback loops R_f/C_f and L_3. The inductors L_1, L_2, and L_3 can provide the function of the inductive peaking.

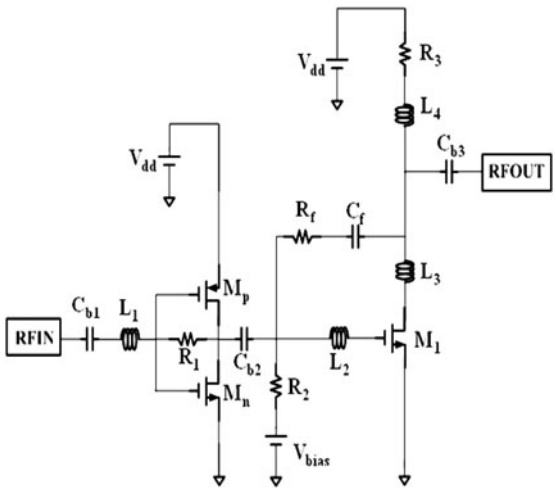

Fig. 5. Schematic representation of the proposed resistive-feedback LNA.

https://doi.org/10.1017/S1759078712000748 Published online by Cambridge University Press

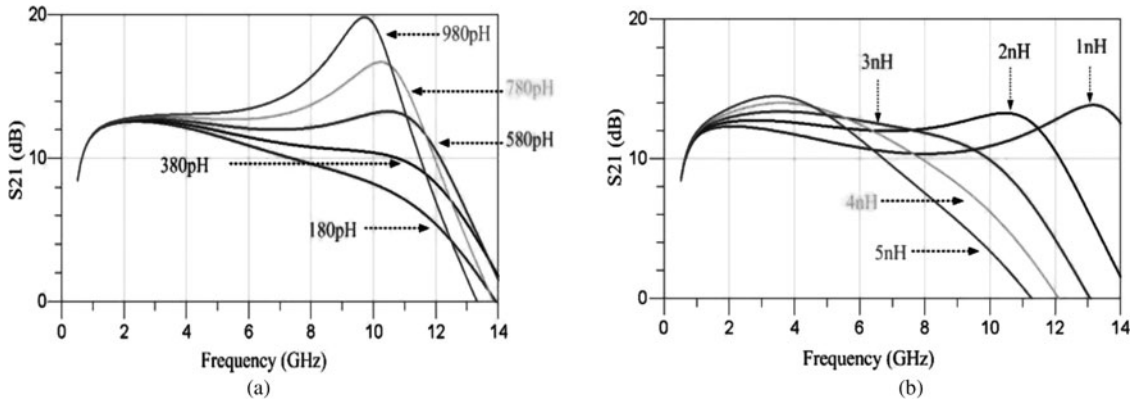

Fig. 6. (a) L_2 peaking inductor effect. (b) L_3 peaking inductor effect.

Table 1. Circuit device size.

Parameters	Devices size
M_p	0.18 × 125 μm ($L \times W$)
M_n	0.18 × 125 μm ($L \times W$)
M_1	0.18 × 112 μm ($L \times W$)
L_1	0.85 nH
L_2	0.63 nH
L_3	1.62 nH
L_4	3.34 nH
C_{b1}	900 fF
C_{b2}	198 fF
C_{b3}	3840 fF
C_f	960 fF
R_1	320 Ω
R_2	3000 Ω
R_3	75 Ω
R_f	460 Ω

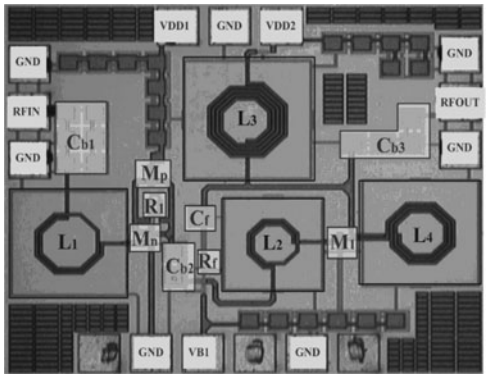

Fig. 7. Layout of the proposed UWB LNA.

Figures 6(a) and 6(b) show the peaking effect with different inductor values. Generally speaking, the property of the input impedance of the transistor can be viewed as capacitive. When the signals go through the transistor, the 3 dB BW will degrade with the capacitive effect. If the inductor is properly chosen and adopted in the circuit, then the 3 dB BW will be expanded by the peaking effect. This phenomenon is shown in Figs 6(a) and 6(b). Here, we choose the value of the inductors L_2 and L_3 as 0.63 and 1.62 nH, respectively. The resistor R_f has

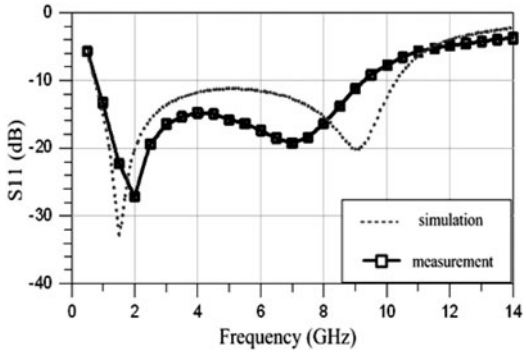

Fig. 8. Simulated and measured results of input return loss (S_{11}).

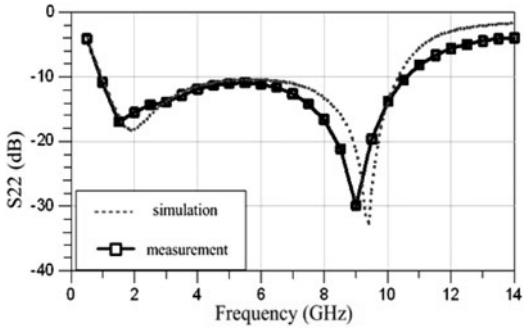

Fig. 9. Simulated and measured results of output return loss (S_{22}).

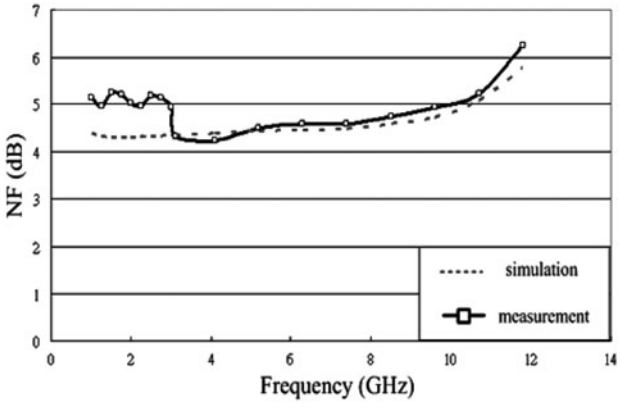

Fig. 10. Simulated and measured results of NF.

https://doi.org/10.1017/S1759078712000748 Published online by Cambridge University Press

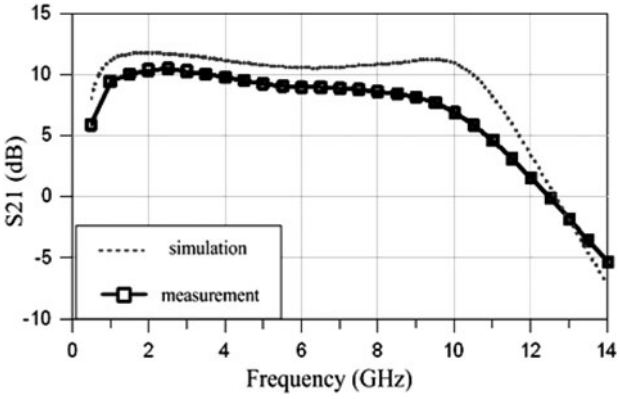

Fig. 11. Simulated and measured results of power gain (S_{21}).

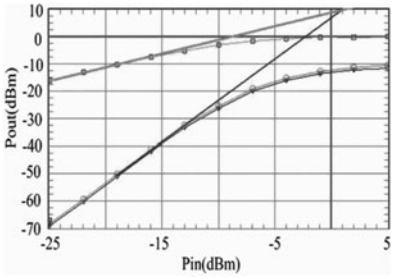

Fig. 12. Measurement of IIP3.

equivalent resistance by the Miller theorem to provide 50 Ω matching. C_{b1}, C_{b2}, and C_{b3} are the block capacitors. The sizes of the circuit devices in the proposed structure are shown in Table 1. The simulations showed that the proposed circuit has a stability factor >2 from 1 to 10.5 GHz.

III. MEASUREMENT RESULTS

Figure 7 shows the die photo of the two-stage wideband amplifier, which has a chip size 0.69 mm². In Fig. 8, it can be seen that the input return loss (S_{11}) is lower than −8 dB, but in Fig. 9 it can be seen that the output return loss (S_{22}) is lower than −10.8 dB from 1 to 10 GHz, respectively. In Fig. 10, it can be seen that the NF is located between 4.2 and 5.2 dB in the whole band. The difference between the simulated and measured data below 3 GHz can be ascribed to the oscillating behavior of S_{11} (see Fig. 8). The power gain whose peak value is 10.5 dB at 2.4 GHz is shown in Fig. 11. The differences between the simulated and measured gain can be ascribed to the parasitic capacitor of the IC pad, which has to be considered in the design process. Moreover, increasing the value of the inductor L_3 could improve the gain performance. In Fig. 12, the third-order input intercept point (IIP3) at 4.98 and 5.02 GHz is 1 dBm. The power consumption is 12.65 mW at 1.5 V supply voltage.

To compare the overall performance of our LNA with the previously published ones, a figure of merit (FOM) that takes into account the gain, F, BW, area, and the DC power consumption of the LNA is defined as [11, 12].

$$\mathrm{FOM}_A = \frac{\mathrm{Gain}_{max}\,(\mathrm{dB}) \times \mathrm{BW}\,(\mathrm{GHz})}{(F-1) \times P_{DC}\,(\mathrm{mW}) \times \mathrm{Area}\,(\mathrm{mm}^2)}, \qquad (6)$$

where BW is the 3 dB BW with frequency of operation in GHz, P_{dc} is the power consumption in milliwatts, and the values of the gain and noise factor F are their absolute values. Area represents the chip area and its value is respective to a typical area of 1 mm².

The performance comparison of the proposed circuit with other reported papers is shown in Table 2. Compared with these amplifiers, this work achieves the third highest FOM_A and the lower-power consumption. For low-power applications, the performance of our work is compatible to other LNAs. The proposed circuit shows a good performance for wideband and low-power applications.

IV. CONCLUSION

We have presented a low-power, wideband CMOS LNA with resistive feedback. The proposed resistive-feedback inverter is employed to achieve wideband input matching and save chip area. The power consumption is 12.65 mW with a 1.5 V supply voltage. In the whole band, the maximum power gain is 10.5 dB and the minimum NF is 4.2 dB. Our work shows a good performance for wideband and low-power applications.

Table 2. Measurement comparison of the familiar topology LNA with other reported LNA.

	[10]	[13]	[14]	[15]	[16]	[17]	This work
Technology (μm)	0.18 CMOS	0.15 pHEMT	0.18 CMOS	0.18 CMOS	0.18 CMOS	0.18 SiGe	0.18 CMOS
Frequency (GHz)	2.8–7.2	3.1–10.6	3.1–10.6	3.1–10.6	3.1–10.6	2–10	1–10
BW_{3dB} (GHz)	2.8–7.2	3.1–10.6	N/A	N/A	1.5–11.7	2–10	1–10
NF_{min} (dB)	3.0	3.4	4.5	4.5	3.74	3.3	4.2
S_{11} (dB)	<−4.5	<−12.0	<−9.5	<−11	<−8.6	<−6	<−8
S_{21max} (dB)	19.1	13	13.2	14	12.8	13	10.5
S_{12} (dB)	N/A	N/A	N/A	N/A	<−26	<−23	<−26
S_{22} (dB)	<−7.5	N/A	N/A	N/A	<−10	<−9	<−10.8
IIP3 (dBm)	−1	N/A	−1.4	−12	−11	−7.5	1
P_{DC} (mW)	32	12.9	23	21	10.34	9.6	12.65
Chip area (mm²)	1.63	2.25	1.42	0.46	0.54	0.88	0.69
FOM_A	1.61	2.84	1.67	6.00	17.19	10.8	6.64

https://doi.org/10.1017/S1759078712000748 Published online by Cambridge University Press

ACKNOWLEDGEMENTS

The authors would like to acknowledge the Taiwan semiconductor manufacture company (TSMC) and chip implementation center (CIC) for the wafer fabrications.

REFERENCES

[1] Ismail, A.; Abidi, A.: A 3 to 10 GHz LNA using a wideband LC-ladder matching network, in Proc. 2004 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers. (ISSCC 2004), 2004, Vol. **1**, pp. 384–534.

[2] Bevilacqua, A.; Niknejad, A.M.: An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers, in Proc. 2004 IEEE Int. Conf. Solid-State Circuits, Digest of Technical Papers(ISSCC 2004), 2004, Vol. **1**, pp. 382–533.

[3] Ellinger, F.; Barras, D.; Schmatz, M.; Jackel, H.: A low-power DC-7.8 GHz BiCMOS LNA for UWB and optical communication, in IEEE MTT-S Int. Digest, June 2004, pp. 13–16.

[4] Shiramizu, N.; Masuda, T.; Tanabe, M.; Washio, K.: A 3–10 GHz bandwidth low-noise and low-power amplifier for full-band UWB communications in 0.25-um_ SiGe BiCMOS technology, in IEEE RFIC Symp. Digest, Long Beach, CA, June 2005, pp. 39–42.

[5] Lee, J.; Cressler, J.D.: A 3–10 GHz SiGe resistive feedback low noise amplifier for UWB applications, in IEEE RFIC Symp. Digest, Long Beach, CA, June 2005, pp. 545–548.

[6] Park, Y.; Lee, C.-H.; Cressler, J.D.; Laskar, J.; Joseph, A.: A very low power SiGe LNA for UWB application, in IEEE MTT-S Int. Digest, June 2005, pp. 1041–1044.

[7] Zhang, F.; Kinget, P.: Low power programmable-gain CMOS distributed LNA for ultra-wideband applications, in IEEE Symp. VLSI Circuits, Digest of Technical Papers., 2005, pp. 78–81.

[8] Bevilacqua, A.; Sandner, C.; Gerosa, A.; Neviani, A.: A fully integrated differential CMOS LNA for 3-5-GHz ultrawideband wireless receivers. IEEE Microw. Wirel. Compon. Lett., **16** (3) (2006), 134–136.

[9] Chao, S.-F.; Kuo, J.-J.; Lin, C.-L.; Tsai, M.-D.; Wang, H.: A DC-11.5 GHz low-power, wideband amplifier using splitting-load inductive peaking technique. IEEE Microw. Wirel. Compon. Lett., **18** (7) (2008), 482–484.

[10] Chen, Y.J.E.; Huang, Y.I.: Development of integrated broad-band CMOS low-noise amplifiers. IEEE Trans. Circuits Syst. I: Regular Papers, **54** (2007), 2120–2127.

[11] Hsu, M.-T.; Hsu, S.-Y.: A low power CMOS LNA for 1–10 GHz application, in Proc. 2009 Asia-Pacific Microwave Conf. (APMC 2009), 2009 pp. 1132–1135.

[12] Gramegna, G.; Erratico, G.: A Sub-1-dB NF $\pm$2.3-kV ESD-Protected 900-MHz CMOS LNA. IEEE J. Solid-State Circuit **36** (7) (2001).

[13] Fang, C.; Law, C.L.; Wang, J.H.: A 3.1–10.6 GHz ultra-wideband low noise amplifier with 13-dB gain, 3.4-dB noise figure, and consumes only 12.9 mW of DC power. IEEE Microw. Wirel. Compon. Lett., **17** (2007), 295–297.

[14] Park, B.; Choi, S.; Hong, S.: A low-noise amplifier with tunable interference rejection for 3.1- to 10.6-GHz UWB systems. IEEE Microw. Wirel. Compon. Lett., **20** (2010), 40–42.

[15] Fu, C.-T.; Kuo, C.-N.; Taylor, S.S.: Low-noise amplifier design with dual reactive feedback for broadband simultaneous noise and impedance matching. IEEE Trans. Microw. Theory Tech., **58** (2010), 795–806.

[16] Lin, Y.S. et al.: Analysis and design of a CMOS UWB LNA with dual RLC branch wideband input matching network. IEEE Trans. Microw. Theory Tech., **58** (2) (2010), 287–296.

[17] Park, Y.; Lee, C.-H.; Cressler, J.D.; Laskar, J.: The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation. IEEE Trans. Microw. Theory Tech., **54** (4) (2006), 1687–1697.

Meng-Ting Hsu was born in Changhua, Taiwan, Republic of China in 1961. He received his B.S. and M.S. degrees from Chung-Yuan Christian University in the Electrical and Electronic Engineering in 1989 and 1991, respectively. Since 1992 he has served as a lecturer in the Electronic Department of the National Yunlin University of Science and Technology (NYUST), and he later obtained a Ph.D. degree from National Chiao-Tung University in Communication Engineering in 2004. In 2005, he was promoted to associate professor and has more than 10 years experience in microwave circuit design. His current research interests are in noise theory application on MMIC and CMOS RFICs.

Shih-Yu Hsu was born in Pingtung Taiwan, Republic of China in 1980. He received his B.S. degree in electrical engineering from Cheng Shiu University of Science and Technology in 2003. He received an M.S. from the National University of Science and Technology in electrical engineering from 2007. His current research interests are in CMOS RFICs.

Yu-Hwa Lin was born in Taichung, Taiwan, Republic of China in 1989. He received his B.S. in electrical engineering from Southern Taiwan University of Science and Technology in 2010. Since then, he had been pursuing his M.S. at the National Yunlin University of Science and Technology in electrical engineering. His current research interest is in CMOS RFICs.

https://doi.org/10.1017/S1759078712000748 Published online by Cambridge University Press