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On the evaluation of the high-frequency load line in active devices

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In this work a de-embedding technique oriented to the evaluation of the load line at the intrinsic resistive core of microwave FET devices is presented. The approach combines vector high-frequency nonlinear load-pull measurements with an accurate description of the reactive nonlinearities, thus allowing one to determine the actual load line of the drain–source current generator under realistic conditions. Thanks to the proposed approach, the dispersive behavior of the resistive core and the compatibility of the voltage and current waveforms with reliability requirements can be directly monitored. Different experiments carried out on a gallium nitride HEMT sample are reported.

Keywords: Integrated-circuit design, Microwave amplifiers, Semiconductor device measurements, Semiconductor device modeling, Time-domain measurements

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I. INTRODUCTION

The power amplifier (PA) is one of the most critical blocks of any wireless transmitter chain. The PA is responsible for boosting the delivered output power while operating with high-power efficiency and preserving the signals' integrity. With the evolution of wireless systems during the last decades, the requirements in terms of output power and efficiency have become stricter. This has forced the investigation of new semiconductor technologies in the microwave context. Particularly, since gallium arsenide (GaAs)-based transistors have reached their limits, the attention has been focused on gallium nitride (GaN)-based microwave active devices [1, 2]. Owing to the wide band gap, GaN provides excellent features for high-power applications in the microwave field and has been recognized as the most promising candidate to reach the output power requirements. However, not being a mature technology, a lot of effort has been put to characterize the behavior of GaN-based devices due to the presence of defects in the materials which strongly influence the performance, like for instance the maximum achievable output power [3, 4]. Moreover, due to reliability issues, it is important to monitor the evolution of the signals exciting the active device. As a consequence, the characterization of the behavior of GaN transistors, as possibly close to realistic operating condition, is a fundamental step. Among the different characterization techniques employed, the one based on high-frequency (HF) nonlinear measurements has attracted the interest of researchers in the last decades. Although it relies on expensive equipment, like the large-signal network analyzer (LSNA) [5], it allows the characterization of any active device under realistic conditions, in the microwave frequency range and under high-power excitations. Load-pull (LP) measurements, or more generally *waveform engineering* [6] techniques, are widely exploited to synthesize realistic source and load terminations to achieve the operating condition that maximizes the output power and the efficiency. As such, the LP technique constitutes a powerful tool not only for the design of PA but also for the dynamic characterization of active devices. However, due to the HF operation, the parasitic network and the reactive nonlinearities shape the load line at the device measurement planes thus hiding the load line at the intrinsic current generator plane. Such information is of great interest in PA design, since all design techniques, from class-A to high-efficiency classes [7], are based on the correct definition of the optimum impedances at the device's intrinsic current source (i.e. the device resistive core [8, 9]). In addition, loading conditions providing similar microwave performance may correspond to load lines, at the intrinsic resistive core, with different shapes, which can show very different robustness in terms of reliability constraints (e.g. breakdown). Consequently, in order to accurately define the optimum condition for device operation, the load lines measured at the accessible terminals have to be shifted back to the resistive-core planes.

The method presented in [8, 9] relies on a low-frequency time-domain LP system which directly provides the load line at the intrinsic resistive core and combines it with a model-based description of parasitic network and strictly dynamic nonlinearities. In this way, the information at the intrinsic device plane is moved toward the extrinsic one. In this work a de-embedding technique starting from vector

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HF measurements is proposed. This technique, combined with an accurate description of the parasitic network and the reactive nonlinearities, allows one to obtain the information about the load line at the intrinsic resistive core directly from large signal measurements performed in the microwave range. The work is outlined as follows: in Section II the proposed technique is described, Section III is devoted to the obtained experimental results and the discussion. Finally conclusions are drawn.

II. THE PROPOSED DE-EMBEDDING PROCEDURE

The approach proposed in this work relies on the model topology reported in Fig. 1. With no loss of generality a common source configuration is considered. The model in Fig. 1 can be divided into two sections: an extrinsic one which accounts for the parasitic network and the intrinsic one which models the active area of the semiconductor device. The latter can be further split into a resistive core that includes the current generators and describes the static and low-frequency I/V characteristics, and a capacitive core that accounts for the purely dynamic contribution to the device current due to reactive effects in the presence of very fast-varying signals. It is worth noticing that, in order to guarantee accurate prediction capability, the capacitive core description should properly account for non-quasi-static effects.

This separation into a resistive and a capacitive core is common in the semiconductor area and is the mostly employed in literature [10–12]. Moreover, two different reference planes are defined within the schematic of Fig. 1. The extrinsic plane defines the measurement plane where the probe tips are physically placed. At this plane, the measured phasors of the voltages and currents include the mixed influence of the active core and the parasitic network. On the other hand, the intrinsic plane delimits the device active area where the performance achievable by a selected technology is defined.

The first step of the proposed procedure consists of shifting the measured spectra up to the intrinsic planes. This step [6, 8, 13] requires an accurate description of the parasitic networks (including the device package) which is obtained through S-parameter measurements by exploiting widely known techniques based on lumped elements approximation (e.g. [14]), or, alternatively, by adopting electro-magnetic simulations of the device layout (e.g. [15]). This step can be accomplished straightforwardly by applying a linear transformation in frequency domain, as expressed in

$$\begin{bmatrix} V_{GS}^{INT}(k\omega_o) \\ I_{GS}^{INT}(k\omega_o) \\ V_{DS}^{INT}(k\omega_o) \\ I_{DS}^{INT}(k\omega_o) \end{bmatrix}_{k=-N\ldots N} = \underline{\underline{M}}(k\omega_o) \begin{bmatrix} V_{GS}^{EXT}(k\omega_o) \\ I_{GS}^{EXT}(k\omega_o) \\ V_{DS}^{EXT}(k\omega_o) \\ I_{DS}^{EXT}(k\omega_o) \end{bmatrix}_{k=-N\ldots N}, \tag{1}$$

where the vector of the extrinsic voltages and currents is transformed through the matrix of the parasitic network $\underline{\underline{M}}$ thus obtaining the vector of the voltages and currents at the intrinsic terminals; k is the harmonic index and ω_o the fundamental frequency. The currents obtained after the transformation (1) can be simply expressed as the vector sum of the contributions coming from the resistive and the capacitive core which are assumed to be strictly in parallel:

$$\begin{bmatrix} I_{GS}^{INT}(k\omega_o) \\ I_{DS}^{INT}(k\omega_o) \end{bmatrix}_{k=-N\ldots N} = \begin{bmatrix} I_{GS}^{R}(k\omega_o) + I_{GS}^{C}(k\omega_o) \\ I_{DS}^{R}(k\omega_o) + I_{DS}^{C}(k\omega_o) \end{bmatrix}_{k=-N\ldots N}. \tag{2}$$

The second step of the procedure consists of separating in (2) the reactive component from the resistive one. Such a step is fundamental in order to obtain the device load line at the resistive core plane (i.e. the current generator plane), which is the plane where all amplifier design techniques are defined. It is worth noticing that, due to the presence of the capacitive core, the knowledge of the electrical quantities at the intrinsic plane does not allow to correctly evaluate the current, and consequently the load line, synthesized at the current generator plane. The de-embedding of the parasitic elements can give just an idea of the resistive core load line, which becomes adequate when the capacitive core contribution can be neglected, which is the case under sufficiently low-frequency operation [6, 13]. As a matter of fact, it is necessary to identify the displacement current contribution in (2). To this aim a model-based description of the nonlinear capacitances has to be exploited, which, under the hypothesis of negligible dispersion of the capacitive core, can be simply identified by adopting standard multi-bias S-parameter measurements [8, 10].[1] In particular, when non-quasi-static effects can be neglected, the intrinsic capacitive currents can be expressed as

$$\begin{bmatrix} i_{GS}^{C}(t) \\ i_{DS}^{C}(t) \end{bmatrix} = \sum_{k=-N}^{N} jk\omega_o \underline{\underline{C}}(v_{GS}^{INT}(t), v_{DS}^{INT}(t)) \begin{bmatrix} V_{GS}^{INT}(k\omega_o)e^{jk\omega_o t} \\ V_{DS}^{INT}(k\omega_o)e^{jk\omega_o t} \end{bmatrix}, \tag{3}$$

where $\underline{\underline{C}}$ represent the matrix of capacitances. Alternatively, a harmonic balance solver can be exploited to obtain the displacement current from the capacitive-core nonlinear model on the trajectory defined by the intrinsic gate and drain voltages. It is worth noticing that, in order to obtain accurate load line estimation at the resistive-core plane, the capacitive-core nonlinear model should also correctly account for

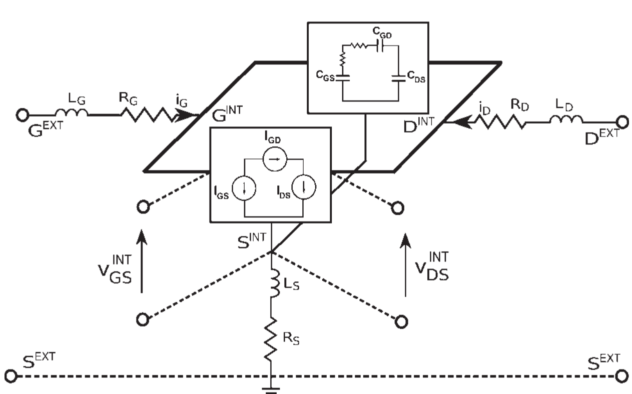

Fig. 1. Equivalent circuit topology as considered in this work.

[1] The capacitive core description can also be obtained by directly exploiting HF large-signal measurements (e.g. [11, 12]).

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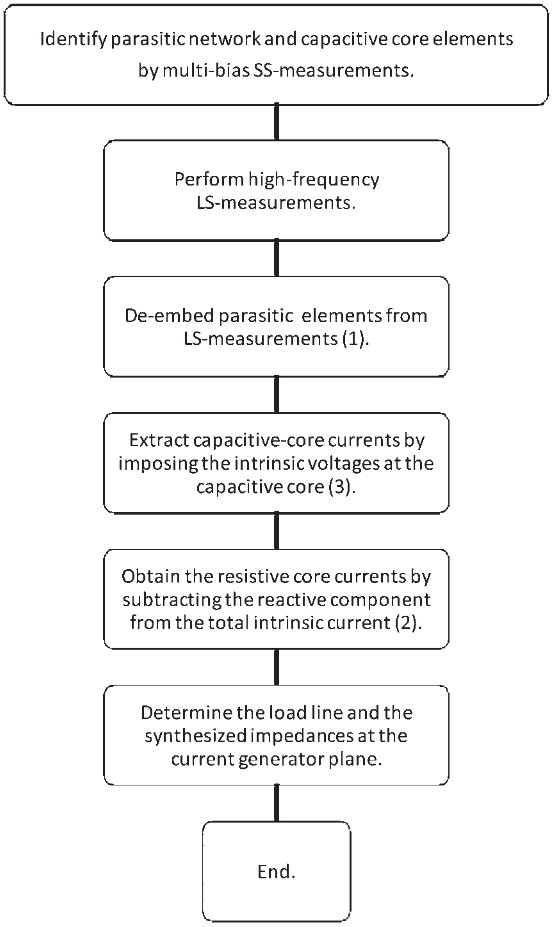

Fig. 2. Flowchart describing the proposed de-embedding technique.

non-quasi-static effects, when these effects play a major role. Once this operation has been carried out the resistive core electrical variables are available, which simply allow one to obtain the load line and the synthesized impedances at the current generator at the fundamental and harmonic frequencies. The flowchart reported in Fig. 2 summarizes the fundamental steps of the proposed de-embedding technique.

It is worth observing that the approach here proposed does not require any optimization procedure by directly providing

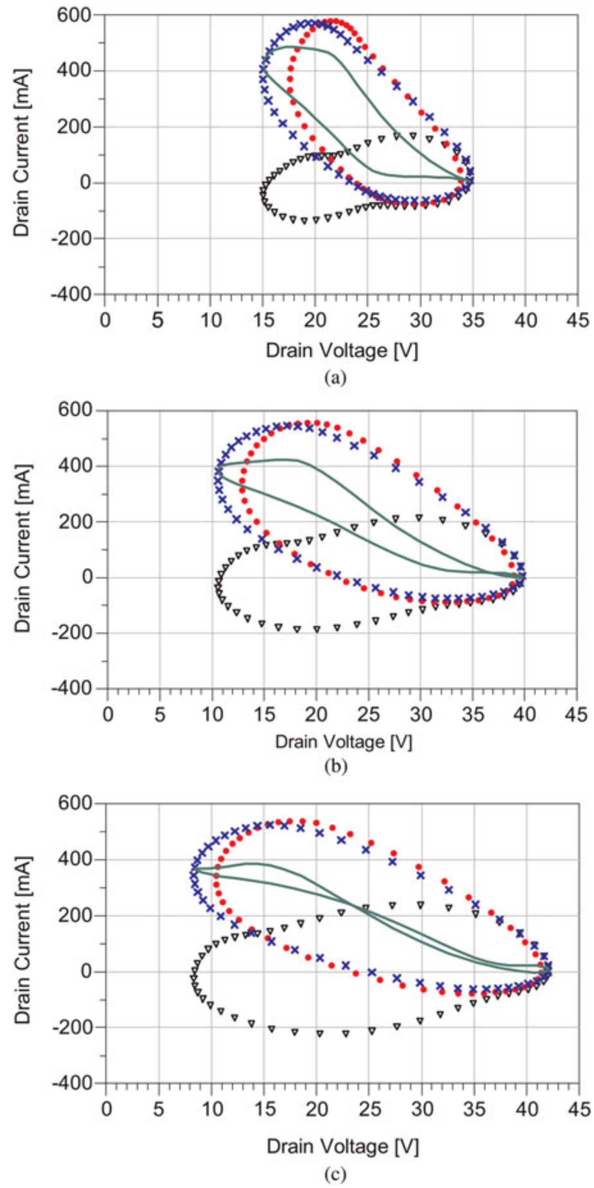

Fig. 4. Measured extrinsic load line (dots), load line after parasitic network de-embedding (crosses), displacement current (triangles), and load line at the intrinsic resistive core (continuous line) at: $V_{GS}^{o} = -2$ V, $V_{DS}^{o} = 25$ V, and $f_o = 4$ GHz. $P_{out} = 0.86$ W (a); $P_{out} = 1.26$ W (b); and $P_{out} = 1.7$ W (c).

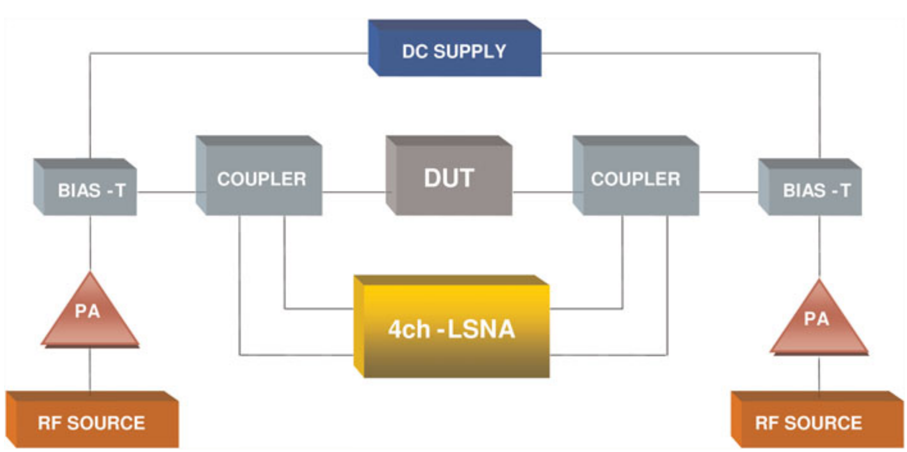

Fig. 3. Simplified block diagram of the measurement system.

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Table 1. Load impedances corresponding to the synthesized load lines for three power levels and up to the third harmonic.

	Frequency		Ext. plane (Ω)	Int. plane (Ω)	Drain current gen. plane (Ω)
P_{out}=0.86 W	f_0	4 GHz	$12.0 + j^*16.9$	$16.3 + j^*20.9$	$29.1 + j^*16.8$
	$2f_0$	8 GHz	$28.3 - j^*16.5$	$28.9 - j^*10.9$	$20.5 - j^*25.1$
	$3f_0$	12 GHz	$58.0 + j^*18.5$	$70.4 + j^*12.4$	$18.5 - j^*27.8$
P_{out} = 1.26 W	f_0	4 GHz	$18.4 + j^*25.2$	$23.5 + j^*29.5$	$47.4 + j^*20.3$
	$2f_0$	8 GHz	$28.1 - j^*16.8$	$28.8 - j^*11.5$	$25.0 - j^*23.7$
	$3f_0$	12 GHz	$54.6 + j^*18.2$	$67.0 + j^*14.0$	$17.4 - j^*26.4$
P_{out} = 1.7 W	f_0	4 GHz	$31.4 + j^*37.7$	$38.8 + j^*42.2$	$82.0 + j^*5.6$
	$2f_0$	8 GHz	$27.8 - j^*17.2$	$28.7 - j^*12.3$	$29.1 - j^*16.9$
	$3f_0$	12 GHz	$53.9 + j^*23.3$	$69.4 + j^*19.5$	$20.4 - j^*26.6$

the information at the current generators plane starting from the HF large-signal measurements. Moreover, by adopting the proposed procedure, the complex low-frequency dispersion phenomena associated to the current generator [6, 16, 17], which are essentially related to the presence of traps and thermal effects, are automatically accounted for.

III. EXPERIMENTAL RESULTS

The effectiveness of the procedure outlined in the previous section has been tested on a GaN HEMT ($0.7 \times 800\ \mu m^2$). Active LP measurements have been carried out by exploiting an LSNA. A simplified schematic of the employed measurement system is illustrated in Fig. 3. The LSNA provides vector calibrated scattered waves in the 600 MHz–50 GHz harmonic bandwidth. HF sources combined with PAs are used to reproduce realistic trajectories and to actively control the termination at the fundamental frequency. The latter is set equal to 4 GHz and the device is biased at $V_{GS}^o = -2$ V and $V_{DS}^o = 25$ V, which corresponds to class-A operation. Different loading trajectories are obtained by varying the phase of the signal injected at the output port thus changing the phase relationship between input and output signals.

In the present case, the parasitic network was extracted by exploiting a conventional technique based on "cold" scattering parameter measurements, while a quasi-static description was found adequate for the capacitive core. In particular, the bias-dependent capacitances were extracted from multi-bias S-parameter measurements and then stored into a look-up table. Experimental results corresponding to load lines for three different values of the output power are reported in Fig. 4. As observable from the figures, the extrinsic load lines are affected by a strong reactive component whose major contribution is due to the nonlinear capacitive core. In fact, for the selected measurement frequency, the linear parasitic network slightly rotates and shrinks the measured load line as confirmed by comparing the extrinsic load line and the transformed one after applying (1). Finally, in Fig. 4, the load lines at the current generator plane, which actually determine the active device performance and represent the theoretical basis of PA design techniques, are shown. It is clear that the combined effect of the parasitic network in conjunction with the capacitive nonlinearities impacts significantly the shape of the load line masking the information relative to the solely resistive core.

In order to demonstrate the impact of the capacitive core on the impedances synthesized at the current generator plane when microwave operation is involved, in Table 1 a comparison between the synthesized impedances at the three different considered planes (i.e. extrinsic, intrinsic, and current generator planes) is reported. The numbers in the table further highlight the importance of shifting the measurements at the current generator plane where the synthesized impedances strongly differ from the one obtained at the measurement plane. As said, the impedances at the current generator plane determine the voltage and current waveforms which can be compared with the theoretical waveforms in order to perform the so-called *waveform engineering* [6].

In Fig. 5 the three load lines at the intrinsic resistive core are reported together with the static characteristic measured at $V_{GS}^o = 0$ V. The marked point on the load lines corresponds to an instantaneous value of the intrinsic gate voltage of 0 V; if low-frequency dispersion was not present these points should belong to the depicted static characteristic. Whereas, as clearly observable, the dynamic I/V significantly deviates from the static characteristics which is the indication of the influence of the thermal effects and the traps [16, 17].

It is worth to observe that the proposed technique can be successfully exploited to perform waveform engineering techniques also in the measurement phase by monitoring the dynamic load line at the resistive core while optimum source and loading conditions are achieved at the accessible extrinsic planes.

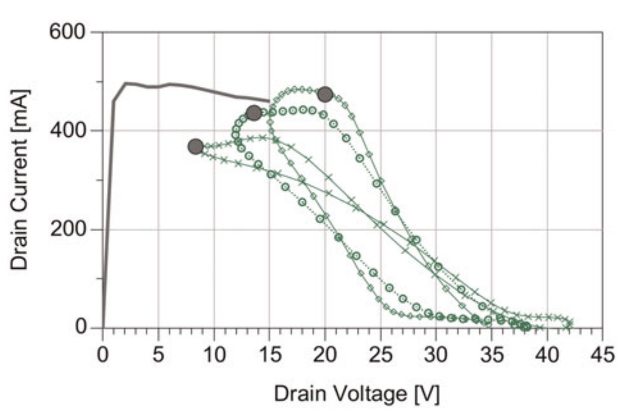

Fig. 5. Load lines at the intrinsic resistive core for the output power values reported in Fig. 4 (symbols) and static characteristic at $V_{GS}^o = 0$ V (continuous line). The marked point on each load line corresponds to the instantaneous gate voltage value equal to 0 V.

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IV. CONCLUSION

In this work a rigorous approach for the evaluation of the load line at the transistor resistive core under nonlinear HF operation has been formulated. The proposed technique allows one to run-time retrieve from HF large signal measurements the actual load line at the drain–source current generator plane. Consequently, direct information about the dispersive behavior of the I/V nonlinearities are inferred. The proposed approach can be applied to any arbitrary extrinsic load line and exploits a model-based description of the reactive nonlinearities. The latter, together with the parasitic networks, can be identified through standard multi-bias S-parameter measurements.

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