RESEARCH PAPER

Design, simulation, and fabrication of broadband coaxial matched loads for the frequency range from 0 to 110 GHz

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Combining a theory for reflection-free termination of coaxial lines together with a novel manufacturing method results in 1-mm coaxial matched loads with an excellent absorption behavior over the frequency range from 0 to 110 GHz. Three different electromagnetic (EM) simulation approaches verify the capability of these matched loads to achieve reflection coefficients smaller than −43 dB over the entire frequency range. Matched loads with a maximum reflection coefficient of only −32 dB have been produced. An excellent performance was achieved by exponentially tapering the outer conductor over the region of a coaxial ceramic substrate coated by a thin-film resistance and by compensation for EM wave propagation inside the resistive coating.

I. INTRODUCTION

Vector network analyzers (VNAs) for coaxial 1 mm systems [1] allowing broadband measurements of scattering parameters from 0 to 110 GHz are an important tool for many radio frequency (RF) engineers. In order to be able to perform precise measurements, the systematic measurement errors of the VNA, as summarized in an error network, need to be determined during a calibration procedure and compensated for in all subsequent measurements.

During the calibration procedure, different characterized calibration standards are connected to the VNA ports. Calibration standards are circuits with certain known properties (dependent on the chosen kind of calibration). The error network can be calculated from the measured reflected and transmitted waves of a test signal and the known properties of the standards.

Calibration at lower frequencies is not possible with calibration techniques such as line reflect line (LRL) [2], thru reflect line (TRL) [3], and offset shorts [4]. At lower frequencies, the phases of the scattering parameters of different line standards or different offset short standards will be too close to each other for adequate separation [5, 6].

For calibration at low frequencies, it is therefore common to apply calibration techniques that use a matched load standard such as open short match (OSM) [7], thru open short match (TOSM) [8], or unknown open short match (UOSM) [9]. The magnitude of the reflection coefficient of a matched load $|S_{11}|$ is related to the achievable calibration accuracy. Especially, if the matched load used for the calibration is not characterized and during the error term correction it is assumed that the matched load does not reflect any electromagnetic (EM) wave. Then the actual value of $|S_{11}|$ directly contributes to the uncertainty of the determined error network. Consequently, larger values of $|S_{11}|$ lead to increased measurement uncertainties.

Previously published matched loads for coaxial 1-mm systems are summarized in Fig. 1. The maximum reflection coefficient over frequency as specified by the manufacturer is assigned to the vertical axis. From the figure, it can be seen that all the matched loads for coaxial 1-mm systems have a relatively large $|S_{11}|$ at higher frequencies and therefore
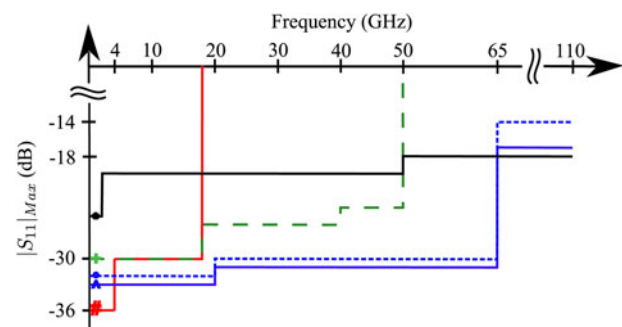
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Fig. 1. Previously published matched loads for coaxial 1-mm systems with their maximum $|S_{11}|$ as specified by the manufacturer: #[10]; ^, °[11]; *, +[12].

lead to increased measurement uncertainties if they are used to calibrate VNAs over the entire frequency range from 0 to 110 GHz.

To avoid using matched loads with larger $|S_{11}|$, it is possible to use lines instead of matched loads with a LRL or TRL calibration technique at higher frequencies [10]. However, a line standard is a beadless air line that consists of two separate parts: an outer conductor and a center conductor. These are very small for coaxial 1-mm systems. It is therefore very time consuming and thus an expensive procedure to connect air lines to the VNA ports. A lot of effort is especially required to perfectly center the inner conductor with respect to the outer conductor.

Also to avoid this problem, it is possible to use the offset shorts technique instead of LRL or TRL at higher frequencies [11]. Nevertheless, each change from one calibration technique to a new one introduces a discontinuity in the determined systematic error terms that will affect all subsequent error-corrected measurements.

The discontinuity can be avoided by collecting redundant measurement information and by applying a statistical analysis [13]. However, each additional calibration standard required for calibration means additional effort during the calibration. The effort can be measured, for example, by the number of electrical connections that need to be set up. A thru and an unknown thru require two electrical connections for connecting their ports to the corresponding VNA ports. An open, a short, and a matched load also require two electrical connections, assuming a two-port calibration is performed where each of the standards has to be connected to each VNA port. For the overdetermined offset calibration technique presented in [12], one thru, one open, one matched load, and four offset shorts are required. This results in 14 electrical connections. When only UOSM or TOSM is used, just eight electrical connections are necessary. This means that collecting redundant measurement information as in [12] results in almost doubling the amount of work involved in the calibration.

From the above discussion it is clear that, because of the lack of a matched load with very good absorption behavior over the entire frequency range, a tradeoff between the calibration effort, discontinuity in the determined systematic error terms, and measurement uncertainty needs to be made.

In this paper, all the mentioned problems are overcome through the design and realization of a matched load with excellent absorption behavior from DC to 110 GHz. Section II presents the theoretical derivation of the matched load design. Section III verifies the derived design and the made assumptions using three different EM simulations approaches. In Section IV, the fabrication process used for the realization of matched loads is presented. The results are discussed in Section V.

II. THEORETICAL DERIVATION OF MATCHED LOAD DESIGN

A) Outer conductor profile in resistance region

The well-known equation for the reflection coefficient S_{11} in uniform coaxial lines with characteristic impedance Z_L terminated by the impedance Z_T is

$$S_{11} = \frac{Z_T - Z_L}{Z_T + Z_L}. \tag{1}$$

From this equation it can be concluded, that for the case that the coaxial line is terminated by an impedance equivalent to the characteristic impedance of the coaxial line,

$$Z_L = Z_T, \tag{2}$$

the reflection coefficient will be zero. The characteristic impedance of the coaxial line Z_L can be calculated as

$$Z_L = \frac{Z_{F_o}}{2\pi} \ln \frac{r}{a}. \tag{3}$$

Z_{F_o} is the characteristic wave impedance, r is the radius of the outer conductor, and a is the radius of the inner conductor (see Fig. 2).

If the resistor consists of a non-conductive substrate covered by a resistive thin film that terminates the inner conductor of the line and has the same radius as the inner conductor, the remaining ohmic resistance $R(z)$ dependent on the remaining part of the resistive layer z (see Fig. 2) can be calculated as

$$R(z) = z \frac{R_o}{l_o}, \tag{4}$$

where R_o is the total resistance and l_o is the total length of the resistor.

In the line region, equation (2) is valid when R_o is equal to the characteristic line impedance Z_{L_o}. To make sure that equation (2) is also valid in the region of the resistance, equation (3) has to be set equal to equation (4) and the required profile of the outer conductor for reflection free propagation
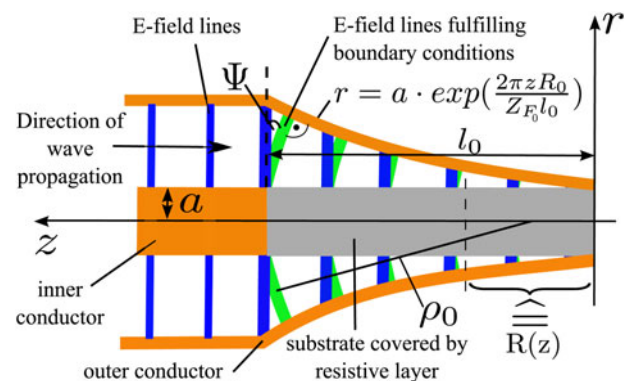

Fig. 2. Matched load with cylindrical substrate covered by a resistive layer and an exponentially tapered outer conductor in the region of the resistive layer. The condition for reflection-free propagation of equation (2) is now valid everywhere, but the boundary conditions for the E-field are violated in the region of the resistive layer. Blue field lines represent the case assumed by using equation (2) and green field lines represent the real situation. a: radius of the inner conductor; r: radius of the outer conductor; z: remaining part of the resistive layer; l_o: length of the resistor; Ψ: loss angle; ρ_o: radius of spherical E-field phase fronts; Z_{F_o}: characteristic wave impedance; R_o: total resistance; $R(z)$: remaining Ohmic resistance.

is described by

$$r = a \cdot \exp\left(\frac{2\pi z R_o}{Z_{F_o} l_o}\right). \tag{5}$$

B) Condition for the use of the derived design

Further considerations on the validity of equation (5) are necessary, since equation (3) is only valid for lines where transverse electromagnetic (TEM) waves propagate. By also using this equation for the region of the resistive layer it is assumed that a TEM wave propagates there as well. The propagation of the TEM wave in the region of the coaxial line and in the region of the coaxial resistance is illustrated by the blue lines in Fig. 2. The assumption of propagation of the TEM wave within the region of coaxial resistance violates two boundary conditions for the E-field. The first violated boundary condition is that the E-field has to be normal to the surface of a perfect electrical conductor (PEC) and thus to the surface of the outer conductor, which usually consists of excellent conducting material and can be assumed as the PEC.

The second violated condition is that the E-field propagating over a resistive film surface will be tilted away from the normal of the surface of the resistive film to the direction of propagation at a loss angle Ψ given by

$$\sin\Psi = \frac{R_\square}{Z_{F_o}}, \tag{6}$$

where $R_\square$ is the sheet resistance given by

$$R_\square = 2\pi \cdot a \cdot \frac{R_o}{l_o} \tag{7}$$

and Z_{F_o} is the characteristic wave impedance. Because of the two generally violated boundary conditions for the E-field (in the same way, two conditions for the H-field are also violated, but it is sufficient to consider only the E-field), the question should be asked if and under what conditions it makes sense to taper the outer conductor exponentially according to equation (5) in order to minimize the reflection coefficient.

This question has been answered in [14] by making the assumption that the E-field phase fronts are spherical (green lines in Fig. 2) with radius ρ_o and that their phase center lies on the z-axis. In this case, all the boundary conditions for the E-field in the resistance region are satisfied if the outer conductor is designed in the form of a tractrix. (Each tangent of the tractrix (outer conductor) cuts the asymptote (z-axis) at the same distance (ρ_o).) Furthermore, it has been proven that as long as the condition

$$\sin\Psi = \frac{R_\square}{Z_{F_o}} = \frac{a}{\rho_o} << 1 \tag{8}$$

is valid, the condition for TEM wave propagation in the resistive region is approximately satisfied and the TEM wave will propagate without any reflection.

In [15], an exact equation for the tractrix profile of the outer conductor has been derived as

$$z = \frac{l_o Z_{F_o}}{2\pi R}\left[\ln\frac{1 - \sqrt{1 - \frac{r^2}{\rho_o^2}}}{\frac{r}{\rho_o}}\right.$$
$$\left. + \sqrt{1 - \frac{r^2}{\rho_o^2}} - \left(\ln\frac{1 - \sqrt{1 - \frac{a^2}{\rho_o^2}}}{\frac{a}{\rho_o}} + \sqrt{1 - \frac{a^2}{\rho_o^2}}\right)\right]. \tag{9}$$

By applying series expansions equation (9) becomes

$$z = \frac{l_o Z_{F_o}}{2\pi R_o}\ln\frac{r}{a} - \frac{l_o Z_{F_o}\sin^2\psi}{8\pi R_o}$$
$$\times\left[\left(\frac{r^2}{a^2} - 1\right) + \frac{\sin^2\psi}{8}\left(\frac{r^4}{a^4} - 1\right) + \frac{\sin^4\psi}{24}\left(\frac{r^6}{a^6} - 1\right) + \dots\right]. \tag{10}$$

When the second part on the right-hand side of equation (10) is negligibly small, which is the case when the already known condition from equation (8) is valid, the obtained expression is exactly equal to equation (5).

To sum up, it can be said that the smaller the sheet resistance is, which means the longer the resistive layer is, the more equation (6) will be valid and the smaller $|S_{11}|$ will be. However, since increasing the length of the resistive layer decreases the mechanical stability, a tradeoff between $|S_{11}|$ and mechanical stability needs to be found.

C) Relative permeability compensation of ceramic substrate

It has been shown [14] that propagation of the wave inside a substrate with relative permittivity $\varepsilon_{r_{sub}}$ causes a reduction of the inductance ΔL of the line in this region according to

$$\Delta L = -\pi\varepsilon_{r_{sub}}\left(\frac{R_o}{l_o}a\right)^2. \tag{11}$$

Up to now, the fact that the conductivity of the resistive layer is finite has been neglected. Owing to the finite conductivity the EM field will penetrate the resistive layer and propagate not only between the outer conductor and resistive layer but also inside the substrate. The case for a coaxial line with uniform outer conductor and one part of the inner conductor consisting of a substrate covered by a resistive layer shown in Fig. 3 has been investigated in [14].

It can be seen that the effect is independent of frequency and can therefore be compensated. A well-known approach to increase the inductance of a line is to increase the distance between the inner and the outer conductor. Thus, either the outer conductor should be designed with a bigger radius b' or the inner conductor should be designed with a smaller
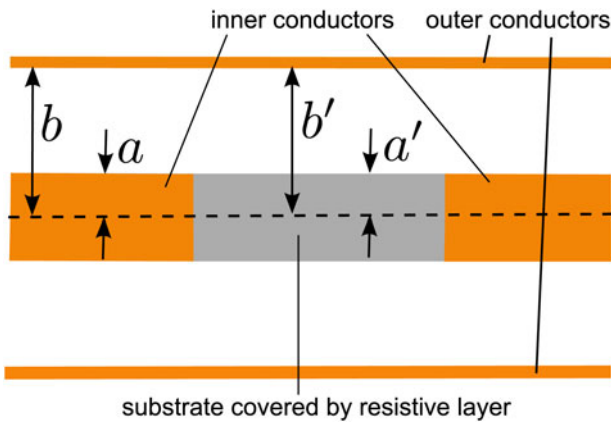
Fig. 3. Uniform coaxial line with one part of the inner conductor consisting of a coaxial substrate covered by a resistive film. a and b are the radii of the inner and outer conductors of the coaxial line. a' is the radius of the substrate and b' is the radius of the outer conductor in the region of the resistive layer required in order to compensate for the reduction of the inductance caused by EM-field propagation inside the substrate.
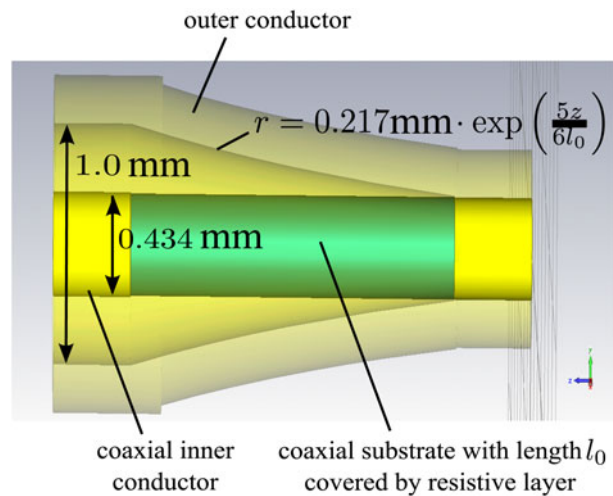

Fig. 4. Model used for the 1-mm coaxial matched load in EM simulations. The diameters of the inner and outer conductors were set according to the IEEE standard [1]. The tapering of the outer conductor was designed according to equation (13). The start value for the substrate radius was chosen according to equation (12).

radius a' according to the formula

$$\frac{a}{a'} = \frac{b}{b'} = 1 + \frac{\varepsilon_{r_{sub}} \sin^2 \psi}{4} \qquad (12)$$

derived in [16]. Although not exactly the same, the similar behavior can be expected for the case that the outer conductor has an exponential profile. The increased inductance for the 1 mm matched load considered in this paper was realized by decreasing the radius of the substrate. The start value of the substrate radius was calculated using equation (12) and fine tuned using EM simulations.

III. EM SIMULATIONS

A) Simulation model

The simulation model was set up according to Fig. 2 and is presented in Fig. 4. The length of the resistive layer was set to some millimeters, as a tradeoff between mechanical stability and $|S_{11}|$. By using the wave impedance of vacuum $Z_{F_o} = 120\pi\ \Omega$, $R_o = 50\ \Omega$ and $a = 0.217$ mm, the outer conductor profile was designed according to equation (5) as

$$r = 0.217\ \text{mm} \cdot \exp\left(\frac{5z}{6l_o}\right). \qquad (13)$$

In order to find the substrate radius that best compensates for the inductance ΔL, simulations with different radii were performed. The start value for the radius was calculated using equation (12). The excellent simulation results with the best substrate radius can be seen in Fig. 5. Here, the maximum $|S_{11}|$ is only -43 dB over the entire frequency range from 0 to 110 GHz, which means that less than 0.7% of the EM wave was reflected.

B) Verification by different simulation approaches

The EM simulation was carried out with three different simulation approaches and two different simulation tools. In all three approaches, a waveguide port that represents an infinitely long waveguide connected to the structure was used for excitation. The inner and outer conductors were modeled as PEC.

In the first simulation approach, CST Microwave Studio [18] with transient solver and hexahedral mesh was used. Even though the real thickness of the resistive layer that covers the cylindrical ceramic substrate is in the range of some tenth of nanometers, it was modeled by a 5 μm thick
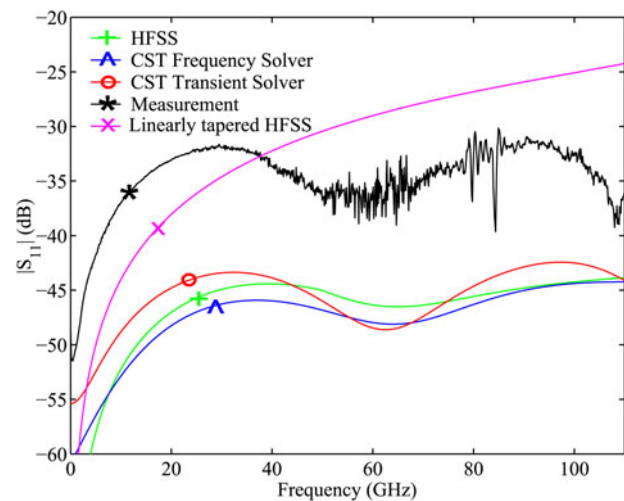

Fig. 5. $|S_{11}|$ simulation and measurement results. The simulation results for a matched load with an exponentially tapered outer conductor performed with different simulation approaches are shown by: + HFSS, ∧ CST Frequency Solver, ○ CST Transient Solver. Simulation result for a predecessor model where the outer conductor was linearly tapered [17] is shown by x. ∗ shows a typical measurement result for a produced matched load with exponentially tapered outer conductor.

layer. The resistivity was chosen such that the overall resistance was 50 Ω. The well-tried approach of using a 5-μm layer instead of the true value for simulations with CST Microwave Studio was used in this work. Before 2011, it was not possible to perform simulations of infinitely thin layers in CST, and the introduction of a resistive layer with a thickness of some hundreds of nanometers would have led to a dramatic increase in the number of mesh cells. By using a 5-μm thick layer and placing at least two mesh cells across the thickness of the resistive layer according to CST guidelines, the number of mesh cells could be kept below five millions.

A hexahedral mesh and a transient solver were used. At discrete locations and at discrete-time samples, the development of the fields over time is calculated by the Finite Integration Technique (FIT). Furthermore, an adaptive mesh refinement setting was used. With this setup, an initial simulation is run using an initial mesh. For subsequent simulations the mesh is refined. The higher the EM fields gradients in an area, the stronger the mesh refinement. The changes in S-parameters (ΔS) from one simulation to the next are compared to the adaptive convergence criteria being ΔS smaller as a certain set value for the entire frequency range from 0 to 110 GHz. At least two simulations have to be performed for the convergence criteria to be met. This setup prevents acceptance of the results of a simulation with an improper mesh.

The second approach used CST Microwave Studio with the frequency domain solver, a tetrahedral mesh and a resistive layer represented by an infinitely thin resistive layer ("Ohmic Sheet Resistance"). When using the CST frequency solver, FIT is still used for spatial discretization. In contrast to the hexahedral mesh, the tetrahedrons of the tetrahedral mesh conform to solid-boundaries, and the mesh refinement can be local with respect to all coordinate directions. The use of an Ohmic Sheet allows assigning a resistance to an infinitely thin layer of material. The EM fields in the simulation have the same magnitude on both sides of the Ohmic Sheet, but their direction in the vicinity of the Ohmic Sheet is determined by the loss angle, dependent on the specified value of the Ohmic Sheet. Thus, the Ohmic Sheet is a very good approximation of reality, where the resistive layer is only some tens of nm thick and determines only the loss angle and can be considered as "transparent" for the EM fields. Furthermore, since the Ohmic Sheet is infinitely thin, no mesh cells need to be placed inside the resistive layer. This means that the smallest mesh cell can be much larger than with a 5-μm thin layer and thus the amount of mesh cells can be kept low. The number of tetrahedrons was about 70 000 and the simulation time was much shorter than with a 5-μm thin layer. An adaptive mesh setting with the same convergence criterion as in the first approach was used.

The third approach was to use Ansoft HFSS [19]. HFSS uses the finite-element method in the frequency domain and tetrahedral meshes to divide the problem space into sub-regions for which Maxwell's Equations are then solved. The resistive layer in HFSS was modeled as infinitely thin. Using the "Lumped RLC Boundary" it is possible to define the resistance R, inductance L, and capacitance C in parallel to any surface. HFSS determines the impedance per square of the surface at any frequency. A resistive layer with properties $R = 50$ Ω, $L = 0$ H, and $C = 0$ F was assigned. The same stop criteria as in the first two simulation approaches were

again used for the adaptive mesh refinement. The results found in [20] stating that the number of nodes on the circumference of the conductor and substrate need to be significantly increased in order to prevent the field simulator from producing modes strongly different from the coaxial TEM mode and thus from falsifying the result, could be confirmed.

The largest difference in the simulation results can be seen between the CST Transient Solver and the other two approaches. This is explained by different methods of modeling the resistive layer. This is also the reason why the number of mesh cells and the simulation time was significantly lower in the last two approaches as compared to the first approach. Furthermore, the simulations performed with HFSS were approximately six times faster than the simulations with CST in the second approach. A simulation result for a predecessor model as presented in [17], where the outer conductor was linearly tapered, can also be seen. It is evident that tapering the outer conductor exponentially instead of linearly significantly improves the performance of the matched load.

IV. FABRICATION PROCESSES

The maximum reflection coefficient of -43 dB over the whole frequency range from 0 to 110 GHz achieved in EM-simulations is a satisfactory result. Therefore, the corresponding simulation model already shown in Fig. 4 became the starting point for the manufacturing model. The manufacturing model involves all the details required by the production process as specified in the engineering drawings. To avoid failures during the transfer of the simulation model to the manufacturing model and in order to investigate the impact of the manufacturing features on the reflection behavior of the matched load, the finished three-dimensional (3D) CAD model of the manufacturing model was imported into EM-simulation tools. The result of the EM simulation of the manufacturing model performed with HFSS can be seen in Fig. 6. The manufacturing features could be implemented with only a minimal increase in the maximum reflection coefficient. The production process for the coaxial 1-mm matched
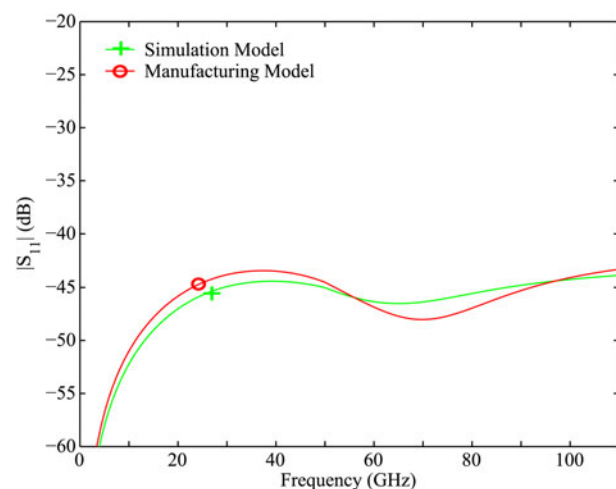

Fig. 6. HFSS simulation results for the manufacturing model compared to the HFSS simulation results of the simulation model shown in Fig. 4. The manufacturing features could be implemented with only a minimal increase in the maximum reflection coefficient.
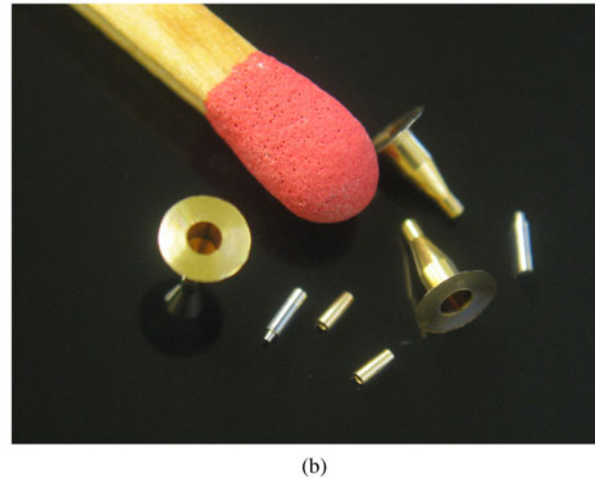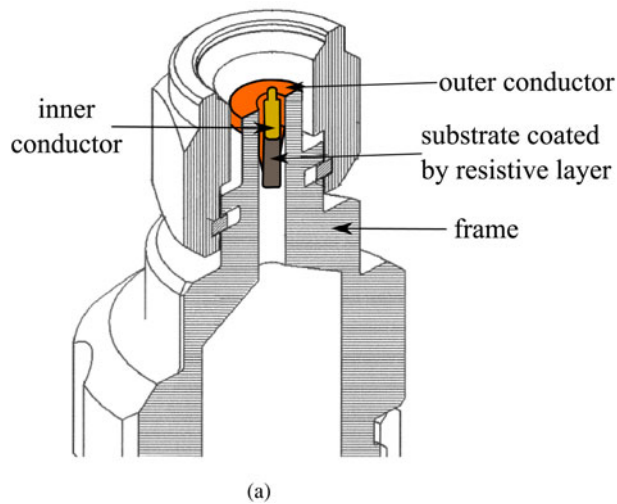
Fig. 7. (a) Geometry of the complete broadband matched load where the outer conductor has already been glued to a frame making the matched load manageable [17]. (b) Single components of the matched load (inner conductors, outer conductors, and coaxial substrates coated by resistive layer) compared in their size to a match.

load with an exponential outer conductor was adapted from [17]. A schematic view of a 1-mm male matched load with a tapered outer conductor can be seen in Fig. 7(a), the individual components in Fig. 7(b). First, the inner conductor consisting of a hard metal is produced by turning. Then, a gold layer is electroplated in order to increase the conductivity. The cylindrical ceramic substrate is produced by mechanical grinding. It consists of hipped Si_3N_4. This material was chosen based on its high bending strength, which makes the substrate resilient to mechanical stress. Furthermore, Si_3N_4 has a small relative dielectric constant that is almost frequency independent and can be compensated for as previously described.

The resistive layer on the substrate is realized by a NiCr alloy. The length of the resistive layer is equal to the length of the exponentially tapered region. The thickness of the alloy is chosen such that the total resistance value is slightly less than 50 Ω. Afterwards a laser trimming process is used to increase the resistance to exactly 50 Ω. The substrate is then soldered to the inner conductor. The production of the outer conductor starts by turning an aluminum part. The aluminum part has the negative form of the desired outer conductor. In the next step, gold is electroplated on the aluminum part to achieve high conductivity of the outer conductor. The thickness of the electroplated gold is chosen such that the outer conductor becomes mechanically stable yet remains slightly elastic. The aluminum part is then etched off and the outer conductor is finished.

The next production step consists of placing the inner conductor unit inside the outer conductor and soldering them together. The cylindrical form of the outer conductor in the region where it is soldered to the inner conductor leads to an exact centering between the outer conductor and inner conductor. To make the matched load manageable and to be able to screw it on the VNA ports, the outer conductor is glued to a frame as shown in Fig. 7(a)). The geometry of the matched load combined with the slight elasticity of the outer conductor allows it to withstand mechanical stress that can be introduced, for example, if the matched load is screwed to a coaxial line or to a VNA port where the inner

conductor is not perfectly centered to the outer conductor, or if it is simply dropped.

V. RESULTS AND DISCUSSION

Finished matched loads were measured with an R&S ZVA 110 VNA [21] with a continuous sweep from 10 MHz to 110 GHz. A typical measurement result for a matched load with an exponentially tapered outer conductor is presented in Fig. 5. It can be seen that the shape of the curve coincides very well with the simulated curve shape.

In order to explain the difference in the magnitude of the simulated and measured $|S_{11}|$ magnitude values, EM simulations were used to investigate the influence of manufacturing tolerances on $|S_{11}|$. The manufacturing tolerances (all in line with the specifications in the IEEE standard for coaxial 1-mm systems [1]) shown in Fig. 8 were swept simultaneously. The simulation results verified that the increase in $|S_{11}|$ can be explained by manufacturing tolerances. This becomes obvious by considering the following simple example. If the diameter of the inner conductor is 5 μm too thin and the diameter of the outer conductor is 5 μm too thick, which is still within the tolerances of [1], the impedance of the line will change by 1.4 Ω and $|S_{11}|$ will increase to -35 dB just because of these two deviations. The conclusion of the investigation is that in order to come even closer to the simulation results, manufacturing tolerances need to be even tighter than the specifications in the IEEE standard [1].

The introduction of a transmission region between the coaxial line and the region of the exponentially tapered outer conductor [15] can be expected to further improve the reflection coefficient even beyond the simulated maximum of -43 dB. The transmission region should be used to bend the planar field of the coaxial line smoothly to the spherical field configuration presented in the region of the resistive layer. Replacing the abrupt change in the *E*-field lines found in the current design (see Fig. 2) with a smooth transition would lead to a further reduction in the maximum reflection coefficient and reduce it even beyond -43 dB.
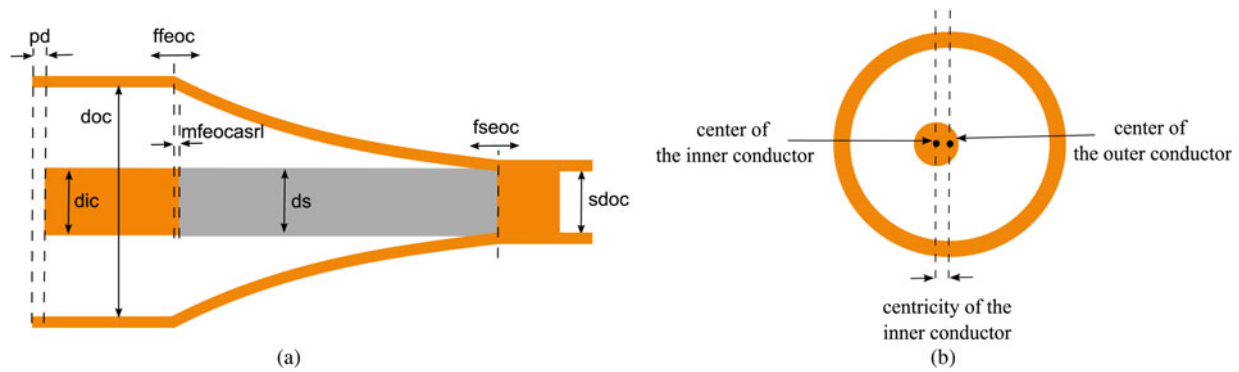
Fig. 8. Manufacturing tolerances whose influence on the matched load's reflection coefficient was investigated using EM simulations. (a) pd: pin depth; ds: diameter of the substrate; dic: diameter of the inner conductor; doc: diameter of the outer conductor; ffeoc: fluctuations in the position of the first edge of the outer conductor; fseoc: fluctuations in the position of the second edge of the outer conductor; sdoc: small diameter of the outer conductor; mfeocasrl: misalignment between the first edge of the outer conductor and the starting point of the resistive layer and (b) centricity of the inner conductor.

VI. CONCLUSION

Matched loads with a maximum reflection coefficient $|S_{11}|$ of -32 dB over the frequency range from 0 to 110 GHz have been produced. Their ability to reach a maximum reflection coefficient $|S_{11}|$ of -43 dB has been verified by EM-simulations. The EM-simulations have been performed in three different ways using two different simulation tools. The differences between the measured and simulated values were explained by manufacturing tolerances swept simultaneously during EM-simulations. The main features of the matched load design are an exponentially tapered outer conductor over a cylindrical ceramic substrate coated with a thin-film resistance, with compensation for EM wave propagation inside the resistive coating. Using such matched loads, it is now possible to calibrate VNAs very accurately with a single OSM, UOSM, or TOSM calibration technique over the entire frequency range, eliminating the time and effort involved in changing to another calibration technique at higher frequencies.

ACKNOWLEDGEMENTS

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