

## RESEARCH PAPER

# Enhanced performance of a 60-GHz power amplifier by using slow-wave transmission lines in 40 nm CMOS technology

XIAO-LAN TANG, EMMANUEL PISTONO, PHILIPPE FERRARI AND JEAN-MICHEL FOURNIER

*This paper shows the contribution of slow-wave coplanar waveguides on the performance of power amplifiers operating at millimeter-wave frequencies in CMOS-integrated technologies. These transmission lines present a quality factor  $Q$  two to three times higher than that of the conventional microstrip lines at the same characteristic impedance. To demonstrate the contribution of the slow-wave transmission lines on integrated millimeter-wave amplifiers performance, two Class-A single-stage power amplifiers (PA) operating at 60 GHz were designed in standard 40 nm CMOS technology. One of the power amplifiers incorporates only the microstrip lines, whereas slow-wave coplanar transmission lines are considered in the other one. Both amplifiers are biased in Class-A operation, drawing, respectively, 22 and 23 mA from 1.2 V supply. Compared to the power amplifier using conventional microstrip transmission lines, the one implemented with slow-wave transmission lines shows improved performances in terms of gain (5.6 dB against 3.3 dB), 1 dB output compression point ( $OCP_{1dB}$ : 7 dBm against 5 dBm), saturated output power ( $P_{sat}$ : >10 and 8 dBm, respectively), power-added efficiency (PAE: 16% instead of 6%), and die area without pads ( $S_{die}$ : 0.059 mm<sup>2</sup> against 0.069 mm<sup>2</sup>).*

**Keywords:** Slow-wave transmission line, CMOS, millimeter-wave, power amplifier

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## 1. INTRODUCTION

Advanced nanoscale CMOS technologies have been largely used to meet the needs of millimeter-wave band applications such as WLAN (60 GHz) and automotive radar (77 GHz) for collision avoidance or microwave imaging, taking the advantages of low cost, low power consumption, compact layout size, and high-level integration into account [1, 2]. Meanwhile, these silicon-based integrated technologies (CMOS 65, 40, and 28 nm) provide the opportunity to integrate active functions such as power amplifiers (PA), thanks to the performance of active components with transition frequency  $f_T$  and oscillation frequency  $f_{max}$  both above 200 GHz [3, 4]. The design of millimeter-wave submicron CMOS power amplifiers is, however, still challenging due to the low-voltage supply (1.2 V) and the significant losses in the passive elements such as transmission lines for matching issue, especially at millimeter-wave frequencies.

The low-quality factor of conventional transmission lines at the operating frequency limits the power gain and saturated output power.

Recently, the Slow-wave Coplanar Waveguides (S-CPW) transmission lines have drawn special attention of scientific community because of its proved potential to obtain high-quality factors [5–10], while providing a wide range of realizable values of characteristic impedances (typically 20–75  $\Omega$ ). Consisting of a conventional coplanar CPW Transmission line (Tline) and a shielded plan formed by floating metallic strips, the S-CPW Tlines become a promising candidate for miniaturization and insertion loss improvement [6, 9]. In 2008, the S-CPW Tlines were first implemented in a low-noise amplifier (LNA) design, demonstrating a good noise figure performance in the K-band range [11].

This paper describes the potential of S-CPW Tlines for the design of millimeter-wave power amplifiers in an advanced 40 nm CMOS technology. In Section II, the optimization of the Tlines, including S-CPW and conventional Thin Film MicroStrip transmission lines (TFMS) will be carried out. Section III is devoted to discuss transistor layout considerations. Finally, in Section IV, two versions of a power amplifier designed with these two different types of Tlines are presented to highlight the contribution of S-CPW Tlines on the overall performance of Class-A power amplifiers.

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II. PASSIVE STRUCTURE: TRANSMISSION LINES

A) TFMS transmission lines

TFMS (Thin Film MicroStrip) Tlines are widely used in the design of millimeter-wave power amplifiers in CMOS technologies [12–18] because of their implementation simplicity. However, the improvement of performance which can be provided by this kind of Tlines is very limited because of its poor quality factor  $Q$  (e.g.  $Q < 10$  in [12]), especially at high frequency. For comparison issue, microstrip Tlines presenting the state-of-the-art performance are simulated with the model developed in [19]. As shown in Fig. 1, the signal conductor strip of the simulated TFMS Tline is made of layer metal 7 and layer AP, the ground plane consists of metal 1 and metal 2 so as to shield completely the high-resistivity silicon substrate [20]. Figure 1(a) shows the cross-section of the 8-metal-layer 40 nm CMOS process from STMicroelectronics foundry used for the design of TFMS and S-CPW Tlines. The Back End Of Line (BEOL) consists of seven copper metals and an aluminum layer (AP). The structure of the classical TFMS Tline used to carry out the amplifiers’ matching network is shown in Fig. 1(b).

B) S-CPW transmission lines

Figure 2 shows the structure of the proposed topology of slow-wave Tline implemented in CMOS technology. This S-CPW

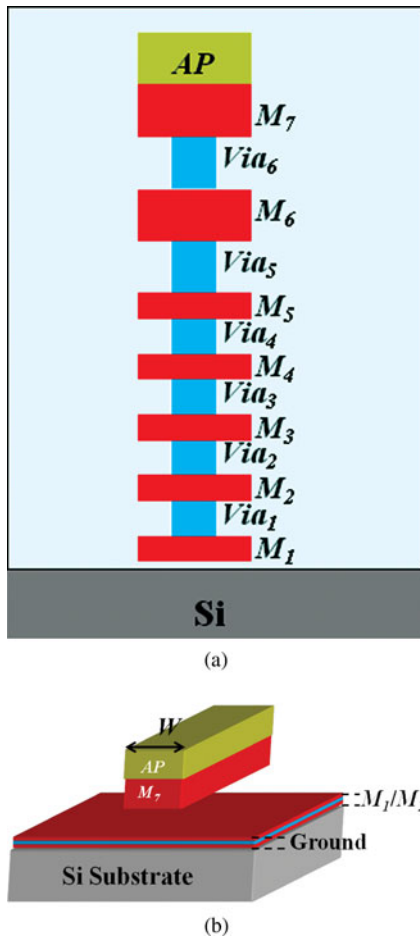


Fig. 1. Schematic description of metal interconnects of 40 nm CMOS technology, (b) structure of a TFMS Tline.

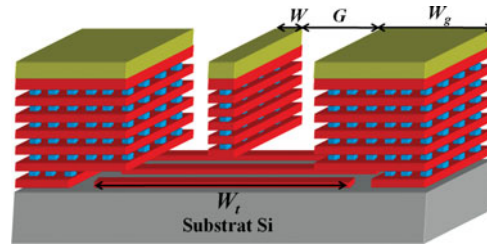


Fig. 2. 3D schematic view of the structure for S-CPW Tline in 40 nm CMOS technology (CPW line on the Metal 2 to Metal 7 + AP and floating strips on Metal 1).

Tline consists of a conventional coplanar waveguide with patterned metallic strips located between the CPW plan and the silicon substrate. These shielding strips are arranged periodically and perpendicularly to the direction of propagation. To ensure the entire isolation from the nearby elements, a new kind of S-CPW Tlines topology, including isolation barriers to shield transversely the propagation structure, is proposed in this paper. The isolation ground planes are realized by stacking all available metal levels from Metal 1 to the top metallic level AP.

1) PRINCIPLE

The effective relative permittivity denoted as  $\epsilon_{reff}$  is defined in equation (1), with  $c_0$  the speed of light in vacuum,  $L_l$  and  $C_l$  the inductance and capacitance per unit length of Tline, respectively.

$$\epsilon_{reff} = c_0^2 L_l C_l \tag{1}$$

The increase in the capacitance, due to the added capacitive effect between the CPW Tline and floating metallic strips, leads to a high effective relative permittivity. The electrical field is mainly confined between the conventional coplanar waveguide and the floating strips, while the spacing between the metallic strips allows the magnetic field going through the substrate, maintaining the value of inductance per unit length  $L_l$  as that of a conventional CPW Tline. The increase in effective relative permittivity then implies an increase in the propagation constant  $\beta$  as described in equation (2), and causes a decrease in physical length of the Tline  $l$  for a given electrical length  $\theta$  by equation (3).

$$\beta = \frac{\omega \sqrt{\epsilon_{reff}}}{c_0} \tag{2}$$

$$\theta = \beta l \tag{3}$$

Moreover, the quality factor  $Q$  (see equation (4)) reflecting the insertion loss of a Tline for a given phase shift is significantly improved.

$$Q = \frac{\beta}{(2 \alpha)} \tag{4}$$

2) OPTIMIZATION OF S-CPW TRANSMISSION LINES

In the S-CPW structure, in order to reduce the conductor losses, the CPW Tline including signal and ground conductor is achieved by stacking all available metal layers except for the

layer Metal 1. The floating metallic strips are laid on Metal 1 because the extreme low thickness of layer  $M_1$  reduces the losses due to the eddy current. The width of signal strip  $W$ , signal-to-ground gap  $G$ , width of ground planes  $W_g$ , total length of each floating strip  $W_t$  of the measured S-CPW line are 7, 19.5, 27, and 66  $\mu\text{m}$ , respectively. The floating strip length and spacing, respectively, denoted as  $SL$  and  $SS$ , have been chosen as the minimum values allowed by the technology ( $SL = 0.1 \mu\text{m}$ ,  $SS = 0.55 \mu\text{m}$ ). Previous studies carried out in [6, 9] have indicated that the insertion loss can be reduced by applying the minimum metal density of the floating strips.

### C) Performance comparison of transmission lines

Slow-wave Tlines were simulated with the 3D EM simulation tool ANSOFT HFSS. To simplify the EM simulation structure and to save the computing time and memory, a method for calculating the equivalent relative permittivity of the multi-layer dielectric developed in [21] was applied.

Figure 3 shows the comparison of the characteristics of Tlines used to design the power amplifiers presented in this paper. For S-CPW Tline, measurements are compared to electromagnetic simulations. Concerning TFMS Tline, the characteristics come from a proposed model [19] based on previous measured TFMS Tlines. The geometric dimensions of the S-CPW Tline have been given in the previous section. The width ( $W = 13 \mu\text{m}$ ) of the microstrip Tline was chosen in order to target the same characteristic impedance as the S-CPW Tline ( $Z_c \approx 25 \Omega$ ). Measurements of the S-CPW Tlines were carried out up to 110 GHz with a LRRM (Line

Reflect Reflect Match) calibration carried out on a network analyzer ANRITSU ME7808C. The characteristic parameters such as the effective relative permittivity  $\epsilon_{\text{reff}}$ , attenuation coefficient  $\alpha$  and quality factor  $Q$  were extracted using the method described in [22], while the characteristic impedance  $Z_c$  was obtained applying another method developed in [23].

The S-CPW shows a measured effective relative permittivity about 12 times greater than that of the TFMS at 60 GHz ( $\epsilon_{\text{reff}} = 48$  for S-CPW against 3.9 for TFMS), resulting in a reduction factor of Tline length greater than 3.5. Thanks to the increased effective relative permittivity (see Fig. 3(b)), the measured quality factor  $Q$  of the S-CPW Tline, shown in Fig. 3(d), is significantly improved compared to the microstrip Tline (about twice at 60 GHz), despite of a higher measured attenuation loss per unit length  $\alpha$  (about 50% higher at 60 GHz).

Let us note the difference between measured and simulated characteristics of the S-CPW Tline. The characteristic impedance exhibits a significant dispersion, a discrepancy of about 20% is observed for the relative effective permittivity of S-CPW, and the simulated attenuation constant is underestimated. These discrepancies are currently under investigation. Concerning the relative effective permittivity, two causes seem to be at the origin of this difference. First of all, as explained above, to simplify the EM simulation of the S-CPW structures, an equivalent relative permittivity was considered for the dielectric layers by using the method developed in [21] for multi-layer dielectric TFMS structures. Secondly, since the thickness separating the CPW and the floating strips, in between layers  $M_2$  and  $M_1$ , is very thin in this technology node, the absolute precision of oxide deposition greatly impacts this thickness precision and consequently the one of the effective relative permittivity. Concerning the attenuation

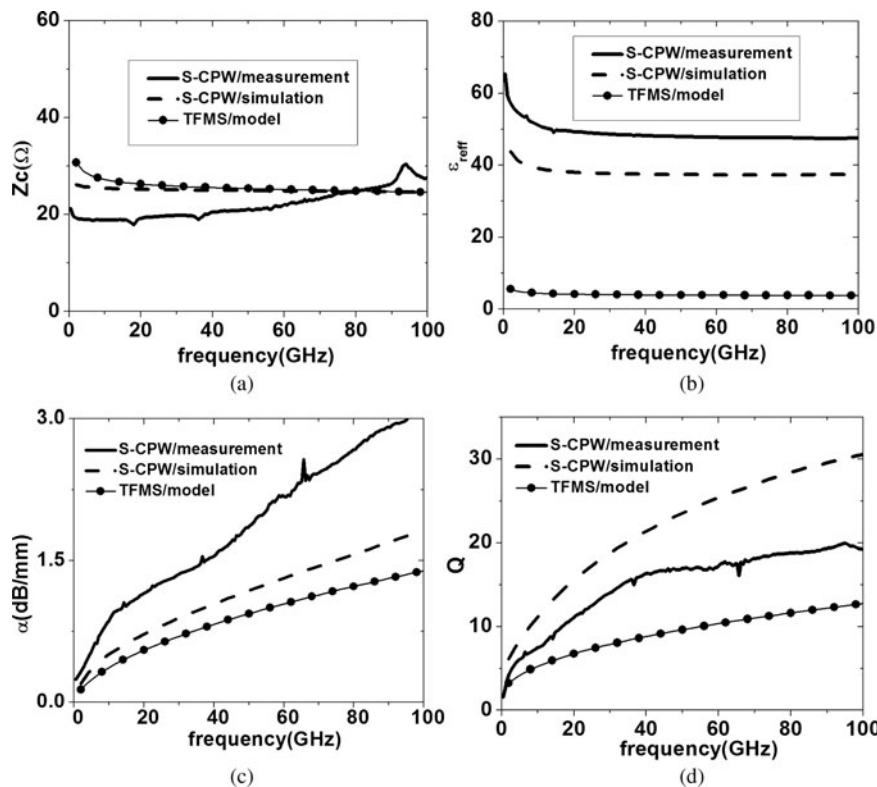


Fig. 3. Performance comparison of the S-CPW and microstrip Tlines: (a) characteristic impedance  $Z_c$ , (b) effective relative permittivity  $\epsilon_{\text{reff}}$ , (c) attenuation constant  $\alpha$ , and (d) quality factor  $Q$ .

constant discrepancy, via holes were not taken into account in the EM simulations to model the stack of the CPW put on the shielded plan of S-CPW. This could explain the underestimation of the attenuation constant.

For the sake of clarity, the measurement results of the S-CPW-based PA are compared in Section IV to both EM simulation, and post-simulation taking into account the S-CPW-measured characteristics.

### III. MILLIMETER-WAVE TRANSISTOR LAYOUT AND DESIGN RULES

The layout of the transistor used in the PAs is shown in Fig. 4. A multi-fingers topology was used to reduce the S/D junction area and the gate resistance. Each drain access of transistor is composed of three stacked metal layers (Metal 1, Metal 2 and Metal 3) to maximize the current flow per finger, meanwhile respecting electromigration rules at 105°C. The number of stacked layers is limited by the parasitic gate-drain capacitance  $C_{gd}$ . The extrinsic model of the transistor taking into account access resistances and parasitic capacitances is obtained, thanks to the post-layout extraction tool (PLS).

#### A) Determination of $W_f$

To determine the optimum value of the width  $W_f$  of each finger, two rules should be taken into consideration as in [24]. Firstly, the maximal current flow  $I_{max}$  as shown in Fig. 4 should respect electromigration rules limit at 105°C, i.e.  $I_{max} = 0.5$  mA/finger. Meanwhile, the amplifier is biased at a current density corresponding to the maximum transition frequency  $f_T$  (i.e. 0.35–0.4 mA/μm) [25–27] to improve the linearity and maximize the saturated output power. The two previous conditions lead to an optimal width  $W_f = 1.3–1.5$  μm ( $= (0.5 \text{ mA}) / (0.35–0.4 \text{ mA}/\mu\text{m})$ ). Finally, the finger was chosen as 1.5 μm.

#### B) Determination of $R_L$

The value of quiescent current for a class-A power amplifier (equation (5)) is  $V_{dd}/R_L$ , where  $R_L$  is the real part of load impedance of the transistor as shown in Fig. 5:

$$I_{ds} = (V_{dd} - V_{ds,sat})/R_L \approx V_{dd}/R_L. \tag{5}$$

The power gain  $G_p$  is defined by equation (6), with  $gm$  the transconductance of transistor and  $Re(z_{in})$  the real part of the input impedance of the MOS, and is proportional to the load impedance  $R_L$ , while the output power  $P_{out}$  (equation (7))

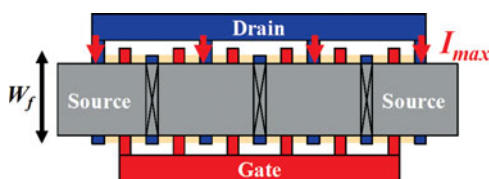


Fig. 4. 2D view of transistor layout.

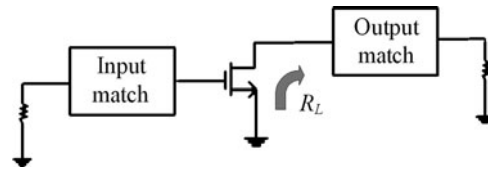


Fig. 5. Simplified schematic for the description of  $R_L$ .

scales with  $1/R_L$ .

$$G_p \propto gm^2 R_L Re(z_{in}) \tag{6}$$

$$P_{out} = \frac{(V_{dd} - V_{ds,sat})^2}{(2 \cdot R_L)} \tag{7}$$

where  $V_{ds,sat}$  is the saturated drain–source voltage.

The determination of optimal value of the load impedance is important to find a targeted trade-off between the power gain and maximum output power of amplifier. Furthermore, load impedance value is limited according to the electromigration rules' constraints. As in [24], Fig. 6 shows the simulated power gain  $G_p$  and the 1 dB output compression point  $OC_{1dB}$  plotted versus the load impedance value for a 60-μm transistor (finger width  $W_f = 1.5$  μm and number of fingers = 40).

For each value of  $R_L$ , the input and output matching are achieved and the class-A behavior of the amplifier is guaranteed. For load impedance smaller than 50 Ω, the electromigration rules at 105°C are not respected anymore since the flowing current is greater than 20 mA (i.e. maximum value for a 40-finger transistor). To obtain a reasonable gain and a good linearity, the best choice is  $R_L = 50$  Ω, corresponding to the limit of electromigration constraint zone (shaded region in Fig. 6). For  $R_L = 50$  Ω, a simulated power gain of 7 dB and output compression point of 8 dBm can be achieved.

### IV. MILLIMETER-WAVE POWER AMPLIFIERS DESIGN

#### A) PA topology

For performance comparison, two versions of a one stage class-A common source power amplifier operating at 60 GHz were designed. One version is implemented with S-CPW Tlines and another with TFMS Tlines as matching

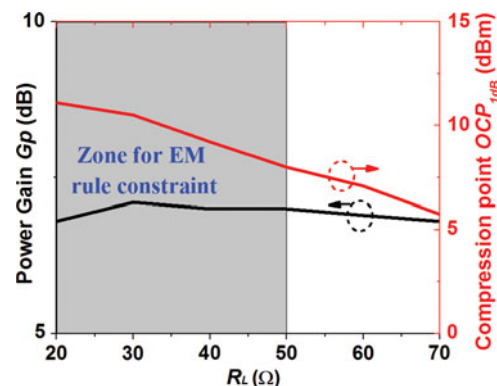


Fig. 6. Simulated  $G_p$  and  $OC_{1dB}$  versus  $R_L$  for 60 μm wide transistor.

networks. Figure 7 shows the simplified schematic of a single-stage power amplifier using the S-CPW Tlines, including the biasing circuits.

The same transistor ( $W = 60 \mu\text{m}$ ) with gate length  $L = 40 \text{ nm}$  was used for both PA versions. The transistor consists of 40 gate fingers ( $N_f = 40$ ), each  $1.5 \mu\text{m}$  wide ( $W_f = 1.5 \mu\text{m}$ ). It was biased at  $V_{gs} = 0.9 \text{ V}$  and  $V_{dd} = 1.2 \text{ V}$ , driving a current  $I_{ds}$  ( $\approx 22 \text{ mA}$ ) corresponding to the maximum transition frequency  $f_T$  ( $\approx 0.35\text{--}0.4 \text{ mA}/\mu\text{m}$ ) and a load impedance  $R_L$  about  $50 \Omega$  for class-A biasing.

The DC blocking capacitors are 3D multifinger MOM (Metal-Oxide-Metal) structures, the value of which is  $200 \text{ fF}$ . In this case, the S-CPW Tlines with a characteristic impedance of  $25 \Omega$  were used as stubs for both input and output matching of amplifier. A low value of characteristic impedance was chosen to obtain a high Q factor, thereby minimizing the total losses in the amplifier. The length of these stubs was calculated to cancel both the imaginary part of input impedance and the output parasitic drain-bulk capacitance. In this way, inputs of the amplifiers are matched to  $50 \Omega$  and outputs are matched to  $R_L$  determined previously (i.e.  $R_L = 50 \Omega$ ). To facilitate the layout connection between the stubs and the transistor of amplifier using S-CPW Tlines, T-shaped junctions were made with the microstrip Tlines. Besides, the extrinsic MOS transistor modeling previously described and the capacitances due to the RF pads for measurement were taken into account in the simulation.

### B) Simulation and experimental results

The simulation results were obtained by using the Cadence software and the simulator tool Eldo from Mentor Graphic. Figure 8 compares the simulated, measured, and post-simulated S parameters of the S-CPW-based PA. As explained above, the simulation considers the electromagnetic model of S-CPW Tline, whereas the post-simulation takes the measured performance of S-CPW Tlines into account.

The maximum simulated gain of this PA is around  $6.5 \text{ dB}$  at  $59 \text{ GHz}$ , which is  $0.9 \text{ dB}$  higher than the measured value. This can be explained by the underestimation of the simulated attenuation loss for S-CPW Tlines, as mentioned in Section II. Moreover, the  $1\text{-GHz}$  working frequency shift between measurement and simulation results is mainly due to the EM modeling of the S-CPW Tline. Indeed, by considering the measured characteristics of the S-CPW Tlines instead of the EM model, post-simulation of the amplifier is in very good agreement with measurement: the difference in maximum power gain at  $60 \text{ GHz}$  is only  $0.2 \text{ dB}$  ( $5.6 \text{ dB}$  measured), and the measured reflection parameters  $S_{11}$  and  $S_{22}$  are both

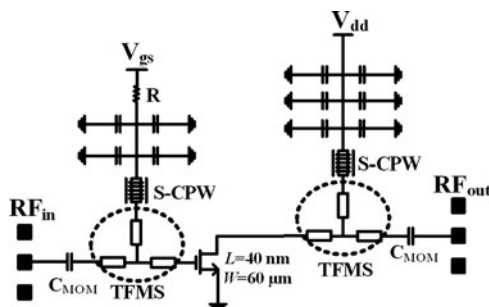


Fig. 7. Simplified schematic of single-stage PA using S-CPW Tlines.

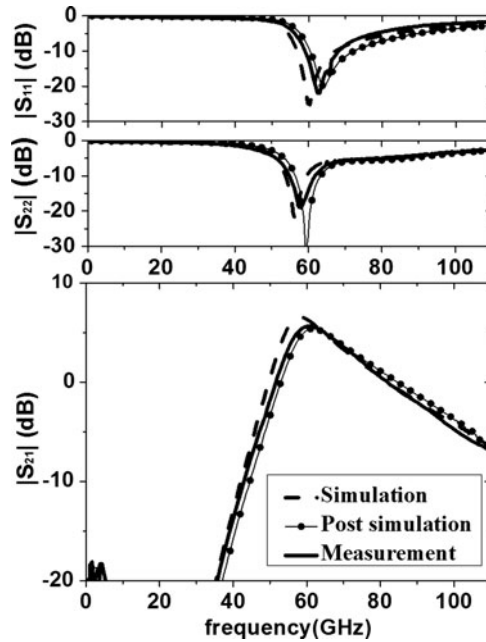


Fig. 8. Comparison of measured and simulated S-parameters of PA using stubs based on S-CPW Tlines.

below  $-10 \text{ dB}$  between  $59$  and  $62 \text{ GHz}$ . This good agreement between post-simulation and measurement allows validating the extrinsic model of the transistor.

Figure 9 shows the S parameters of the TFMS-based PA. The measured maximum gain reaches  $3.3 \text{ dB}$  at  $65 \text{ GHz}$ . In comparison with simulated results, the frequency shift is due to the no-accurate simulated value of the phase coefficient  $\beta$  of TFMS Tlines, which were not fabricated and measured in the same run (limited by the fabrication cost). This amplifier is also broadband and the measured reflection parameters  $S_{11}$  and  $S_{22}$  are both below  $-10 \text{ dB}$  between  $59$  and  $65 \text{ GHz}$ .

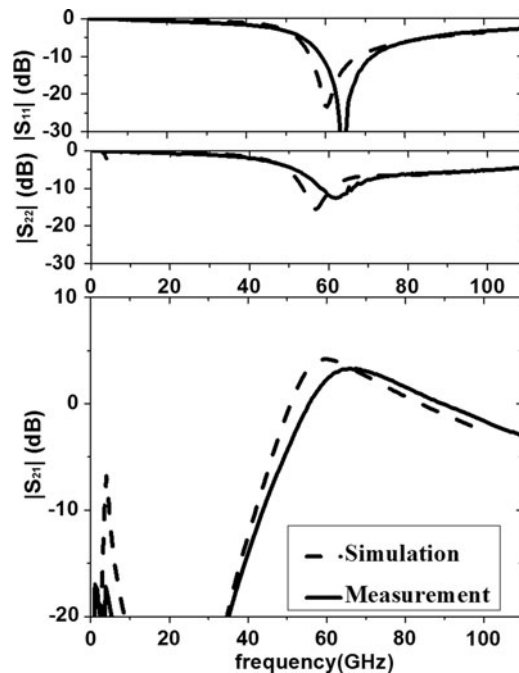


Fig. 9. Comparison of measured and simulated S-parameters of PA using stubs based on microstrip Tlines (TFMS).

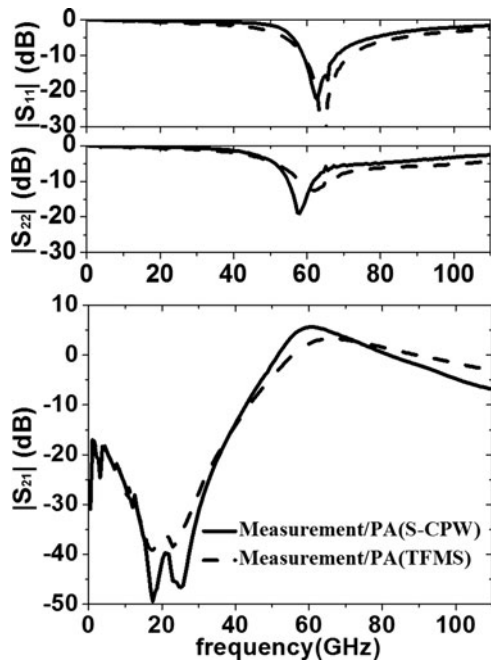


Fig. 10. Comparison of gain performance of the two power amplifiers.

Figure 10 shows the measured performance difference between these two amplifiers with an increase in favor of the S-CPW-based PA with a 3.3 dB improved gain compared to TFMS-based PA. One can observe that resonances appear at low frequencies for both amplifiers. This is due to parasitic inductance of decoupling capacitors at the end of stubs in the drain access, but these resonances magnitudes are smaller than -17 dB.

As shown in Fig. 11, the amplifiers are both unconditionally stable over the entire measured frequency range, from 40 MHz to 110 GHz, with stability factor  $k$  (equation (8)) greater than unity and absolute value of determinant  $|\Delta|$  of S parameters (equation (9)) smaller than unity.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} S_{21}|} \tag{8}$$

$$|\Delta| = |S_{11} S_{22} - S_{12} S_{21}| \tag{9}$$

The measured and simulated large signal results of the two amplifiers are shown in Fig. 12, showing a very good agreement for both amplifiers. At 60 GHz, the amplifier using the

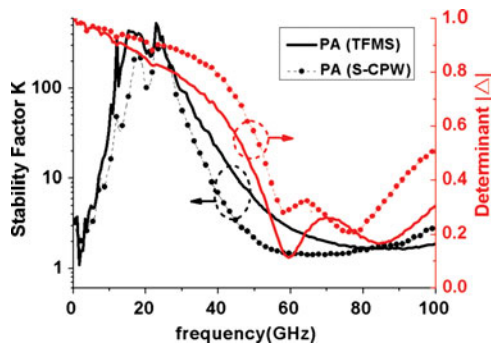


Fig. 11. Measured stability factor and determinant of S-matrix of amplifiers.

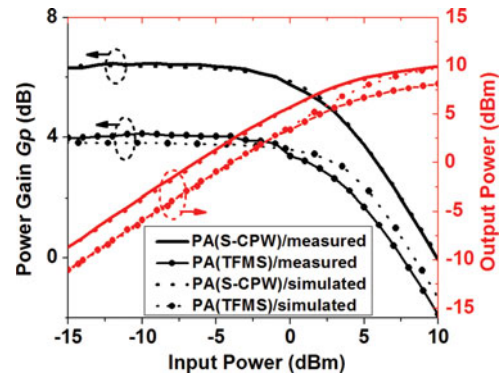


Fig. 12. Comparison of measured and simulated  $OCP_{1dB}$  and  $P_{sat}$  of PA using S-CPW Tlines (@ 60 GHz) and PA using TFMS Tlines (@ 65 GHz).

S-CPW Tlines presents a measured 1-dB output compression point  $OCP_{1dB}$  of 7 dBm, only 0.4 dB lower compared to the simulation. For the amplifier using microstrip Tlines, the measured  $OCP_{1dB}$  at 65 GHz is 5 dBm (6.5 dBm simulated). The output power at saturation ( $P_{sat}$ ) is greater than 10 and 8 dBm, respectively. The measured Power Added Efficiency (PAE) is plotted in Fig. 13. The PAE of the amplifier using the waveguides-CPW Tlines reaches 16%, while the one using microstrip Tlines is limited to 6%.

The performance of both 60 GHz class-A PAs are summarized and compared in Table 1.

Another aspect of the contribution of S-CPW Tlines is shown in Fig. 14. The active area of the amplifier without PADs achieved with the S-CPW Tlines is about 20% less than that based on the microstrip Tlines. The active surfaces  $S_{die}$  are  $0.059 \text{ mm}^2$  (S-CPW) and  $0.069 \text{ mm}^2$  (TFMS), respectively.

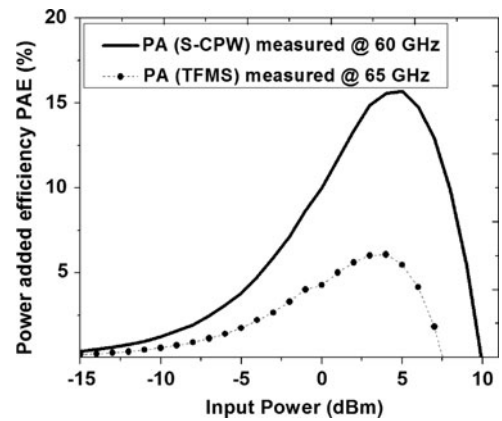


Fig. 13. Measured power-added efficiency of both amplifiers.

Table 1. Comparison of measured performance of the two PAs.

	Frequency (GHz)	Gain $ S_{21} $ (dB)	$P_{sat}$ (dBm)	$OCP_{1dB}$ (dBm)	PAE (%)
PA (S-CPW)	60	5.6	>10	7	16
PA (TFMS)	65	3.3	>8	5	6

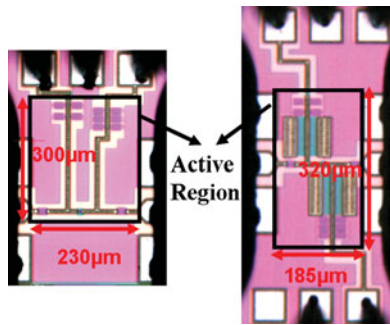


Fig. 14. Die photomicrograph of the PA using TFMS Tlines ( $230 \times 300 \mu\text{m}$ , left) and S-CPW Tlines ( $185 \times 320 \mu\text{m}$ , right).

## V. CONCLUSION

S-CPW Tlines showing high-Q factor ( $\approx 18$  at 60 GHz) have been used in a 40 nm bulk CMOS technology to improve the performance of power amplifiers. The performances of these S-CPW Tlines compared to conventional microstrip Tlines have been highlighted, in terms of quality factor  $Q$  and miniaturization factor since a reduction factor of 3.5 was obtained with the S-CPW Tlines. Hence, to show the contribution of these Tlines, two single-stage common-source 60-GHz power amplifiers using, respectively, S-CPW Tlines and classical TFMS Tlines were implemented in the same technology for comparison. The measured results show that the integration of S-CPW Tlines in the design of power amplifiers provides an overall improvement in performance, in terms of power gain  $G$  (5.6 dB against 3.3 dB), 1 dB output compression point  $\text{OCP}_{1\text{dB}}$  (7 dBm against 5 dBm), PAE (16% against 6%), saturated output power  $P_{\text{sat}}$  (10 dBm against 8 dBm) and layout size ( $0.059 \text{ mm}^2$  against  $0.069 \text{ mm}^2$ ). Besides, the EM simulation tools and design methodology taking the extrinsic model of the MOS into account have also been validated.

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