International Journal of Microwave and Wireless Technologies, 2009, 1(2), 127–136.
doi:10.1017/S1759078709000075 Printed in the United Kingdom

Behavioral modeling and linearization of a millimeter-wave power amplifier

ILAN MELCZARSKY[1], PERE L. GILABERT[2], VALERIA DI GIACOMO[3], EDUARD BERTRAN[2] AND FABIO FILICORI[3]

The use of digital predistortion for linearizing a millimeter-wave power amplifier (PA) is investigated. A PA operating at 38 GHz is designed using an accurate non-quasi-static transistor model, taking into account both short- and long-term memory effects. A realistic test signal is then used for the identification of a nonlinear auto-regressive moving average (NARMA) behavioral model of the PA. The NARMA-based digital predistorter is then derived and formulated in terms of basic predistortion cells, especially suitable for efficient implementation in an FPGA. The performance of the predistortion solution is preliminarily assessed by means of computer simulations.

Keywords: Behavioral modeling, Linearization, Memory effects, Millimeter wave, Power amplifier, Predistortion

Received 21 July 2008; Revised 30 January 2009; first published online 12 May 2009

I. INTRODUCTION

Modern telecommunication standards make use of multilevel and/or multicarrier modulation schemes in order to accommodate high information rates in a limited bandwidth and to provide immunity to channel distortion and multipath effects. Spectral efficiency and immunity to channel conditions, however, are achieved at the expense of a high peak-to-average ratio (PAPR) transmitted signal and of a high sensitivity to intermodulation distortion (IMD). IMD is normally generated by nonlinear dynamic effects in the power amplifier (PA) at the end of the transmission chain. Moreover, the modulation process and PA nonlinearity generate out-of-band distortion, which must remain inside the mask specified by the communication standard. If no linearization scheme is adopted at the transmitter, the only way of meeting the in-band and the out-of-band distortion requirements for signals with high PAPRs is to operate the PA at a high level of backoff, which normally results in poor power efficiency. On the contrary, if the proper linearization scheme is used, significant improvements in system performance and costs can be obtained. In this paper, we address the linearization of a millimeter (mm)-wave PA using digital baseband predistortion [1–3]. Possible applications include current mm-wave high-bandwidth applications such as the bidirectional satellite service at Ka band, IEEE 802.16-SC, LMDS, Point-to-Point Microwave Service and Private Operational Fixed Service (i.e., TV Broadcast, 38.6–40.0 GHz), HAPS, Amateur Radio (licensed), and defense applications. To this aim, and to preliminarily test the validity of the approach, we employed a circuit-level model of a PA operating at 38 GHz, which is based on a simple yet accurate non-quasi-static model of a GaAs pHEMT device. Computer simulations were then performed in order to identify a nonlinear auto-regressive moving average (NARMA) behavioral model for the PA from which the predistorter was derived. The predistortion function, also of NARMA type, was expressed as a combination of basic predistortion cells (BPCs) in order to be efficiently implemented in an FPGA, which is normally already present in most digital transmitters. The performance of the proposed solution was then evaluated for different single- and multi-carrier modulation schemes using computer simulations.

The rest of the paper is organized as follows: section II presents a review of linearization techniques, section III describes the device model and the main considerations made in the design of the mm-wave PA chosen for linearization, section IV presents the NARMA behavioral model used to represent the PA in the predistortion solution, section V describes the predistortion solution, and section VI presents validation results obtained from computer simulations with different modulated test signals.

[1]Dipartimento di Ingegneria Elettronica (DEIS), University of Bologna, Viale Risorgimento 2, 40136 Bologna (BO), Italy. Phone: +39 0512093847; Fax: +39 0512093847; Emails: ilan.melczarsky@unibo.it, fabio.filicori@unibo.it
[2]Department of Signal Theory and Communications, Polytechnic University of Catalonia (UPC), Av. Canal Olímpic s/n, 08860 Castelldefels, Barcelona, Spain. Phone: +34 934137000; Fax: +34 934137032; Emails: plgilabert@tsc.upc.edu, bertran@tsc.upc.edu
[3]Dipartimento di Ingegneria, Università di Ferrara, Via Saragat, 1, 44100 Ferrara (Fe), Italy. Phone: +39 05322093494; Fax: +39 0532974870; Email: valeria.digiacomo@unife.it
Corresponding author:
I. Melczarsky
Email: ilan.melczarsky@unibo.it

II. PA LINEARIZATION

A number of linearization solutions have been proposed in the literature [4]. However, an optimal linearization technique does not exist and so the choice of the linearization scheme is strongly dependent on the application and on a number of factors such as the linearity requirements, the complexity added by the linearizer (and the trade-off between accuracy and complexity), the signal bandwidth, the technology used (e.g., analog or digital), the power efficiency requirements, the

robustness against system changes, etc. Feedback-type linearizers (Envelope, Cartesian, Polar) have been extensively used in the past and are still used in specific applications (e.g., circuit level linearization). However, stability problems make them unsuitable for current high-bandwidth applications. In addition, feedback linearizers reduce overall system gain, which can affect system efficiency. On the other hand, they are less sensitive to disturbances or changes in the transmitter subsystem and therefore good IMD cancellation can be achieved for low or moderate signal bandwidths. Different from feedback linearizers, Envelope Elimination and Restoration and the outphasing techniques (LINC, CALLUM) have revived thanks to the use of current high-speed digital signal processors (DSPs), which have permitted one to overcome certain drawbacks associated with analog circuitry. One of the biggest challenges of these techniques is with respect to power efficiency, since power losses associated with the combination of the signal components can in some cases outweigh the benefits of employing highly efficient PAs. On the other hand, the processing speed of current DSPs limits the linearization bandwidth, although this may change in the future as processing speed improves. Feedforward together with digital predistortion linearization are the most suitable linearization techniques to cope with wideband signals. Feedforward linearization is unconditionally stable, can achieve effective cancelation of IMD, and is immune to PA memory effects. However, its open-loop nature makes it sensitive to possible unbalances in cancelation loops, effectively degrading the overall linearity performance whenever imperfect cancelation occurs. This can be compensated by means of a proper loop control, but it requires additional circuitry. Moreover, the error amplifier and the losses associated with the output combiner strongly impact on the IMD cancelation performance and on overall power efficiency. Analog predistortion is a simpler solution with respect to digital predistortion, but although it can cope with high bandwidths, it only gives moderate IMD suppression. Moreover, analog solutions operating at RF are very sensitive to the electrical lengths in the circuit, which become critical for mm-wave applications. A similar dependence on implementation maladjustments appears in LINC transmitters, due to the need for a good equilibrium between the PA in the two branches. Digital predistortion performed at baseband can achieve better correction capabilities (it is independent of the final carrier frequency of operation) than analog solutions and can be adaptive, thus allowing for corrections of possible unexpected unbalances. The main drawbacks are related to power consumption associated to the DSP device and bandwidth limitations due to the speed of the DSP. Since DSPs are currently present in most communications transmitters for codification and digital modulation purposes, digital baseband predistortion can be a good linearization solution for a high-bandwidth mm-wave application such as the one we are considering, especially when memory effects in the PA are of significant importance in IMD cancelation performance.

III. PA DESIGN

To avoid the uncertainties associated with high-frequency prototyping and measurements, and thus to be able to concentrate on the performance of the PA behavioral model and predistortion scheme, it was decided to preliminarily validate the linearization approach using an accurate circuit-level description of the PA. Accordingly, the main goal in the design of the PA was to obtain a realistic mm-wave PA which was, at the same time, computationally efficient even with complex modulated signals.

This section describes the main characteristics of the PA and the considerations made during the design. The first part presents the non-quasi-static device model that was employed, whereas the second part illustrates the main features of the PA.

A) Non-quasi-static device modeling

To obtain a realistic circuit-level model of a high-frequency PA, an accurate device model is needed that is capable of accounting for short-memory (i.e., non-quasi-static) effects occurring at high frequencies [5]. Moreover, for non-constant envelope applications, low-frequency dispersive effects need to be accounted for. Besides accuracy in predicting the device behavior, the numerical efficiency of the model is also important, as it will be used with complex modulated signals and simulated in the mixed, time-frequency, envelope domain. This section briefly describes the nonquasi-static equivalent-voltage model (NQS-EVM) [5] of a FET device, which was used to account for nonlinear short memory effects at the intrinsic active device of the PA. Long-term memory effects were accounted for by the empirical model described in [6].

The NQS-EVM model is an empirical electron device model featuring a reliable identification procedure and a simple CAD implementation. It also provides good prediction capabilities up to very high frequencies under mildly nonlinear operation. Although the model is technology independent and can be implemented using either look-up tables (LUTs) or equivalent circuits, only the LUT-based version for FET devices will be considered in the following.

The basic idea of the model is to use an associated QS device controlled by suitably defined equivalent voltages: in such a way, NQS effects arising at high frequencies are modeled by means of voltage perturbations imposed by the equivalent voltage sources.

In QS conditions, the behavior of an intrinsic FET device can be simply described by the well-known voltage-controlled equations:

$$\mathbf{i}(t) = \mathbf{F}[\mathbf{v}(t)] + \mathbf{C}[\mathbf{v}(t)]\frac{\mathrm{d}\mathbf{v}(t)}{\mathrm{d}t}, \tag{1}$$

where $\mathbf{i}$ and $\mathbf{v}$ are the vectors of the port currents and voltages, respectively, and $\mathbf{F}$ and $\mathbf{C}$ are purely algebraic functions. At high frequencies, NQS phenomena, which are ignored in (1), become important. We define suitable equivalent voltages $\hat{\mathbf{v}}_c$ and $\hat{\mathbf{v}}_d$:

$$\hat{\mathbf{v}}_c(t) \doteq \mathbf{v}(t) + \Delta\mathbf{v}_c(t), \tag{2}$$

$$\hat{\mathbf{v}}_d(t) \doteq \mathbf{v}(t) + \Delta\mathbf{v}_d(t), \tag{3}$$

in order to provide the proper NQS currents in a virtually QS device described by (1) when the actual controlling voltages are replaced with the equivalent voltages:

$$\mathbf{i}(t) = \mathbf{F}\{\hat{\mathbf{v}}_c(t)\} + \mathbf{C}\{\hat{\mathbf{v}}_d(t)\}\frac{\mathrm{d}\hat{\mathbf{v}}_d(t)}{\mathrm{d}t}. \tag{4}$$

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

In particular, the equivalent voltage domain can be obtained according to (1) by means of the voltage perturbations $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$, which take into account all the fast dynamics of the NQS phenomena.

General considerations and empirical evidence described in [5] suggest that a linear dependence can be assumed for $\Delta\mathbf{v}_d$ and $\Delta\mathbf{v}_c$, that the two voltage perturbations are not mutually independent, and that in the case of a strictly intrinsic GaAs pHEMT the voltage perturbations appear only in series to the gate. In such a way, just two voltage corrections, linearly voltage dependent, account for all NQS effects, according to Fig. 1.

Provided that the duration of memory effects is short with respect to the period of the operating signals, a "modified" dynamic Volterra-series approach [7] can be adopted to model the voltage perturbations, which, by discretizing the memory time in N_D time slots $\Delta\tau$, can be written by means of linear discrete convolutions:

$$\Delta v_{GS,d}(t) = \sum_{p=1}^{N_D} a_{1p}[v_{GS}(t - p\Delta\tau) - v_{GS}(t)] + \sum_{p=1}^{N_D} a_{2p}[v_{DS}(t - p\Delta\tau) - v_{DS}(t)], \quad (5)$$

$$\Delta v_{GS,c}(t) = \rho\Delta v_{GS,d}(t). \quad (6)$$

The dependence on the dynamic voltage deviations $\mathbf{v}(t - \tau) - \mathbf{v}(t)$ allows for a vanishing contribution of (5) and (6) when the signal frequencies involved are not high enough for NQS effects to manifest.

B) Model identification and validation

The first part of model identification involved the derivation of the "strictly intrinsic" device measurements. These were obtained by de-embedding the measured S parameters at the extrinsic ports both from the extrinsic parasitic elements and from all the linear capacitances in parallel to the intrinsic device. Parasitic elements were, in this case, identified through standard cold-FET procedures in pinched-off conditions, and also was the purely capacitive parallel network. The strictly intrinsic measurements were then used in order to identify the quasi-static device and the non-quasi-static voltage corrections.

The chosen device was a 0.25 μm GaAs pHEMT having 10 fingers and 600 μm of total gate periphery. In this case, a LUT-based definition was chosen for the associated quasi-static device both for the conductive currents and for the displacement currents. The conductive currents include a low-frequency dispersive term that accounts for self-heating and surface trap level states, and is modeled using an empirical approach proposed in [6]. The quasi-static capacitive currents are modeled through nonlinear LUT-based capacitors that are identified from the imaginary part of the strictly intrinsic admittance parameters, in a frequency range where reactive effects are evident, but non-quasi-static phenomena are still negligible.

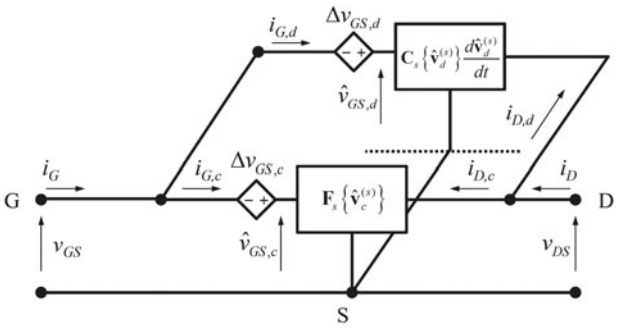

Fig. 1. Topology of the NQS-EVM model.

The second part of model identification concerns the identification of parameters a_{1p}, a_{2p}, and ρ, defining the non-quasi-static voltage corrections. This was achieved by resolving a simple overdetermined system of equations based on

$$\mathbf{Y}(\mathbf{V}, \omega) = \mathbf{G}(\hat{\mathbf{V}}_c)\left[\mathbf{1} + \rho\sum_{p=1}^{N_D}\mathbf{a}_p(e^{-j\omega p\Delta\tau} - 1)\right] + j\omega\mathbf{C}(\hat{\mathbf{V}}_d)\left[\mathbf{1} + \sum_{p=1}^{N_D}\mathbf{a}_p(e^{-j\omega p\Delta\tau} - 1)\right], \quad (7)$$

which gives the strictly intrinsic bias-dependent admittance parameters in the frequency domain and which is derived by inspection of Fig. 1 and simple algebraic manipulations. For the device considered, a total memory length of 1.8 ps divided into three elementary delays gave good results. Equation 7 was evaluated over a reduced bias grid (V_{GS}: −1.2 to −0.2 V; V_{DS}: 2–10 V), so as to have maximum accuracy over the region defined by the dynamic load curve of the device in large-signal operation of the PA. Moreover, in order to properly identify the non-quasi-static corrections, (7) was evaluated in a frequency range covering both quasi-static and non-quasi-static phenomena (3.5 GHz $< f <$ 76 GHz).

Figure 2 shows some small-signal validation results that refer to the intrinsic admittance parameters Y_{11} and Y_{21} up to twice the fundamental frequency of the PA (76 GHz) with the device biased at the nominal quiescent point of the PA (V_{GS}: −0.55 V; V_{DS}: 6.5 V). The figures show the measured and modeled parameters, as well as the results that would have been obtained if a conventional quasi-static model had been employed. As can be seen from the figures, for this bias condition where the device is very conductive, the behavior at high frequencies is far from quasi-static and is accurately accounted for by the model thanks to the voltage-controlled dynamic deviation generators. Similar results are obtained for Y_{12} and Y_{22}, which however are less affected by non-quasi-static phenomena. On the contrary, for bias conditions where the device channel is pinched-off, an almost quasi-static behavior is observed (not shown here due to lack of space) and the model is still able to predict it owing to the fact that it was identified at the strictly intrinsic ports.

Figure 3, instead, shows, for the fundamental frequency of the PA (38 GHz), the measured and modeled admittance parameters as a function of the bias voltages in the region where the model was identified. As can be seen from the figures, even if bias-independent coefficients were assumed for the dynamic deviation generators, the model is able to predict the measured parameters inside a relatively large area of operation for the device including off- as well as on-state conditions.

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

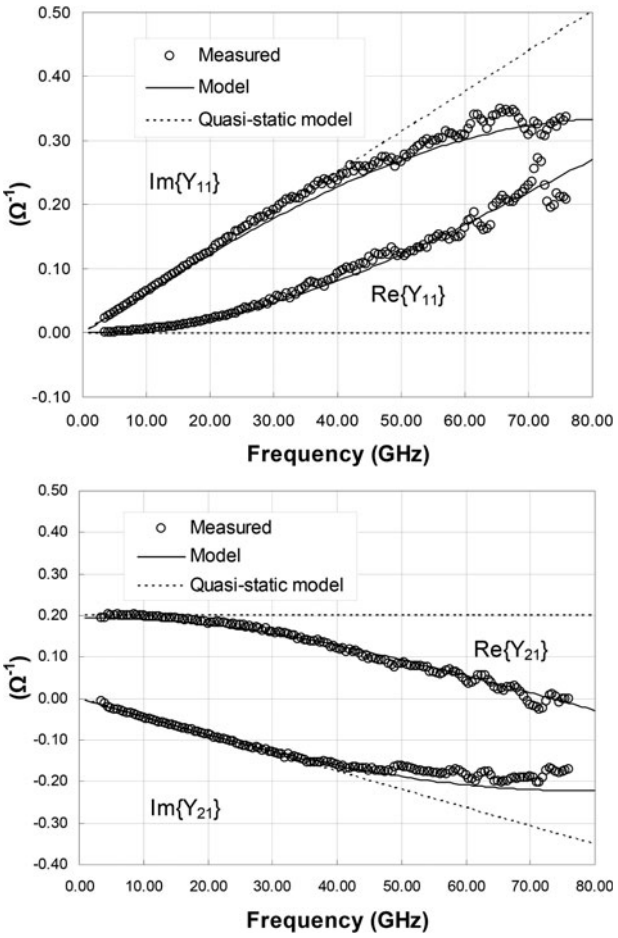

Fig. 2. Measured and modeled intrinsic Y parameters (V_{GS}, V_{DS}) = (−0.55 V, 6.5 V) exhibiting non-quasi-static behavior. Results obtained with a quasi-static model are included for comparison.

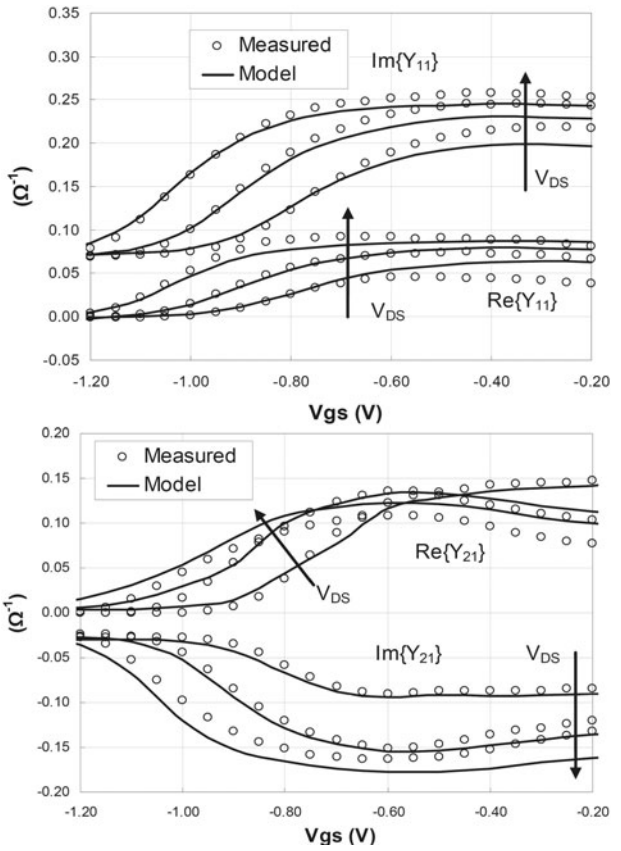

Fig. 3. Measured and modeled intrinsic Y parameters at 38 GHz for V_{DS} = 2, 6.5, and 10 V.

C) Model implementation

After the identification procedure, the model was implemented in an Agilent ADS CAD environment, as shown in Fig. 4 for the intrinsic device. The conductive currents, including low-frequency dispersive effects due to traps and self-heating, are modeled using LUTs and the empirical low-frequency model described in [6].

The displacement currents of the quasi-static device are modeled with nonlinear LUT-based capacitors and implemented using a symbolically defined device. The purely dynamic voltage corrections applied to both conduction and displacement parts of the quasi-static device are implemented through standard linear VCVSs, which depend on intrinsic port voltages and on model parameters a_{1p}, a_{2p}, ρ, $\Delta\tau$, and N_D, which were previously identified. A linear parallel capacitive network separates the strictly intrinsic from the intrinsic device ports, and the standard lumped parasitic network depicted in Fig. 5 is embedded in order to obtain the extrinsic device ports.

D) Power Amplifier

This section describes the design of an integrated mm-wave PA using the non-quasi-static device model identified and implemented in the previous sections. In keeping with the objective of obtaining an efficient yet realistic circuit-level model of the amplifier, a single-stage single-cell PA was considered, which can represent the typical output stage of a real mm-wave PA. Due to linearity requirements, class-AB operation was selected, and the device was biased at 35% of IDSS. The load and source impedance were optimized taking into account IMD and gain, using a two-tone source- and load-pull measurement setup and were also validated with simulations using the non-quasi-static device model [5]. Matching networks were synthesized using distributed networks, as would be the case in any integrated PA operating at such a frequency. Figure 6 shows a schematic of the designed PA and Table 1 reports its main performances.

High-frequency PAs typically exhibit both short- and long-term memory effects due to electrical and thermal phenomena [8], which generally make their linearization more difficult. Any realistic PA model, therefore, needs to account for these effects as they will have an impact in the design and performance of the predistorter. In the application under consideration, however, and taking into account that the signal bandwidth even for very high bit rate communication standards is in the order of tens of MHz, and that therefore the relative bandwidth is small with respect to an mm-wave carrier, only long-term[1] memory effects become important.[2]

[1]Long with respect to the period of the carrier but not necessarily with respect to the period of the smallest frequency of the baseband envelope.

[2]Short-term memory effects in the device must still be accurately modelled in order to predict PA performances related to the high-frequency carrier such as gain, output power, etc.

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

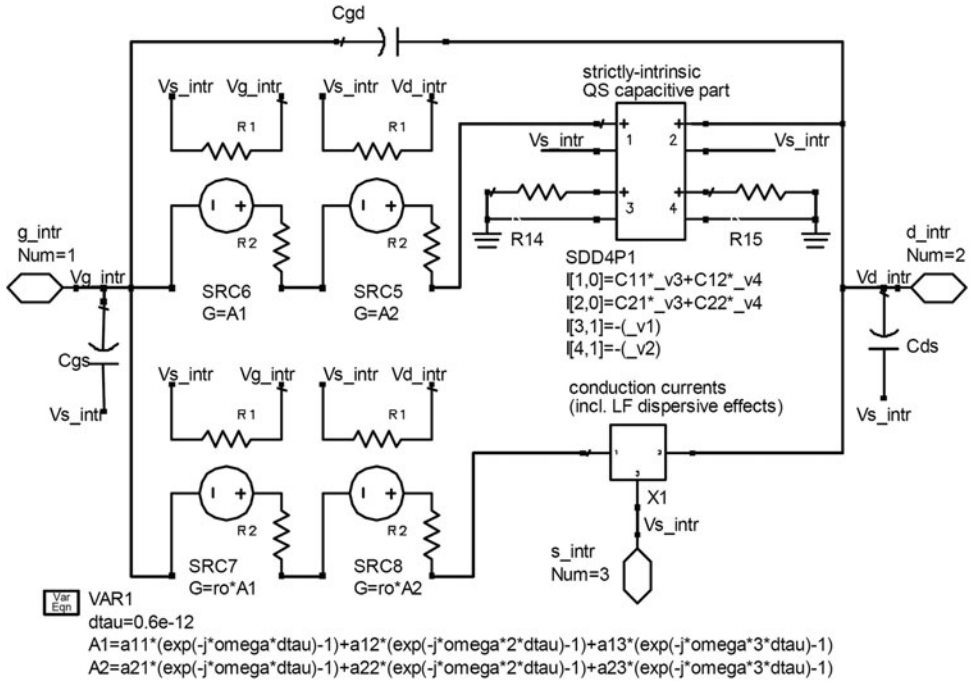

Fig. 4. CAD implementation of the non-quasi-static device model at the intrinsic ports including displacement (top) and conductive low-frequency-dispersive currents (bottom). Non-quasi-static effects are accounted for by dynamic-deviation-based VCVSs. A purely capacitive linear network separates the "strictly intrinsic" ports from the intrinsic ones.

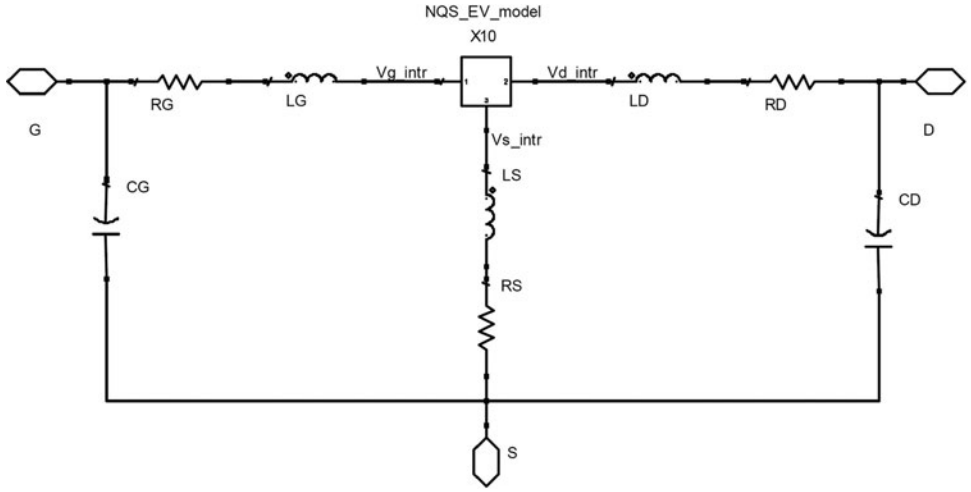

Fig. 5. Parasitic linear network embedded onto the intrinsic device to obtain the extrinsic ports.

This is so because the response of the matching networks and the device are substantially flat over such a small relative bandwidth and therefore they do not exhibit any dynamic effects. Long-term memory effects, instead, are generally associated with thermal phenomena, surface charge traps in the active devices, and low-frequency dispersive bias circuits. The first two were modeled by the low-frequency part of the NQS model whereas bias networks effects were accounted for by careful design of the bias circuit. In fact, if ideal bias networks are considered, long-term memory effects are hardly noticeable, and, as shown in Fig. 7, the two-tone IM3 term is almost independent of tone spacing (for tone spacings up to 20 MHz). The same figure also shows that when a more realistic bias system is considered, not only the IM3 terms depend on tone spacing but also some asymmetry between the left and right IM3 terms appear, as is typically observed in real PAs. This variation dependence over such a narrow frequency range is a symptom of long-term memory effects.

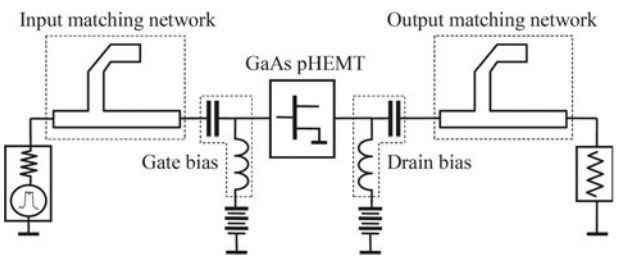

Fig. 6. Schematic of the designed mm-wave PA.

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

Table 1. Main performances of the power amplifier.

Parameter	Value
Small-signal gain	6.9 dB
Bandwidth (−2 dB)	37.5 GHz–38.5 GHz
Output power (I/C: −38 dBc)	14.5 dBm
Gain (I/C: −30 dBc)	6.5 dB
Output power (1 dBc)	18.0 dBm

IV. BEHAVIORAL MODELING

The PA is a nonlinear dynamic system whose memory effects can be of significant importance when wideband signals are considered. The digital predistortion (DPD) linearization technique can compensate for both nonlinear and dynamic PA unwanted effects. The DPD technique requires nonlinear dynamic behavioral models capable of reproducing the PA nonlinear behavior as well as its memory effects. In the last few years, a significant number of behavioral models for PAs have been proposed, as discussed in [9]. However, to be suitable for DPD purposes behavioral models not only need to be accurate enough to mimic PA behavior but also have to be invertible and computationally efficient.

For our particular application, a NARMA model, described in [10], was chosen as a good compromise between accuracy and computational efficiency. The NARMA model can be seen as an extension of a simpler nonlinear moving average (NMA) model that incorporates a nonlinear auto-regressive block. The advantage of using a NARMA model is the introduction of a nonlinear feedback path (infinite impulse response – IIR – terms) that may allow one to relax the number of delayed samples considered to model the PA, in comparison with a model using only finite impulse response (FIR) terms.

One of the main weaknesses of the NARMA model regards its stability. The use of nonlinear feedback paths can derive in the overall system instability. Fortunately, the stability of a NARMA model can be studied and guaranteed using a technique based on the small-signal gain theory, which is advanced in [10]. Figure 8 depicts the block diagram that describes the NARMA model.

The general input–output mathematical expression in a NARMA model can be described as

$$\hat{y}_{\mathrm{NARMA}}(k) = \sum_{i=0}^{N} f_i(x(k-\tau_i)) - \sum_{j=1}^{D} g_j\big(\hat{y}(k-\tau_j)\big), \qquad (8)$$

with $f_i(\cdot)$ and $g_j(\cdot)$ being nonlinear memoryless functions, and where τ_i ($\tau_0 = 0$) and τ_j ($\tau \subset \mathbb{N}$) are the most significant sparse delays of the input and output, respectively, contributing to the description of the PA memory effects. Further details on how to obtain the best sparse delays to characterize the PA dynamics can be found in [11, 12].

By considering memoryless nonlinear functions $f_i(\cdot)$ and $g_j(\cdot)$ characterized by polynomials of order P,

$$f_i(x(k-\tau_i)) = \sum_{p=0}^{P} \alpha_{pi} x(k-\tau_i)|x(k-\tau_i)|^p, \qquad (9)$$

$$g_j(\hat{y}(k-\tau_j)) = \sum_{p=0}^{P} \beta_{pj} \hat{y}(k-\tau_j)|\hat{y}(k-\tau_j)|^p, \qquad (10)$$

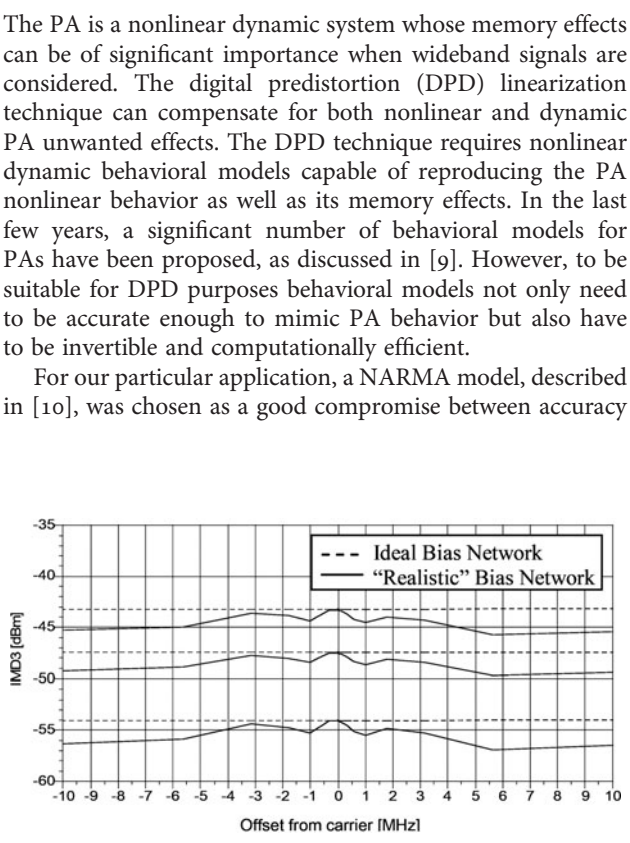

Fig. 7. PA two-tone IMD tests for different input powers and bias systems.

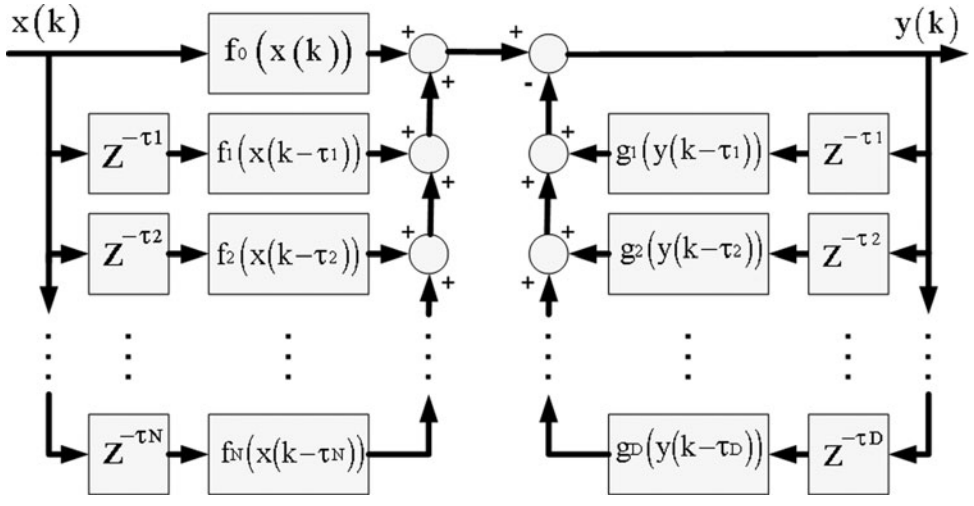

Fig. 8. NARMA model structure.

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

it is possible to rewrite (7) in a more compact matrix notation:

$$\hat{y}_{\mathrm{NARMA}}(k) = \hat{y}(k) = \hat{\boldsymbol{\delta}}^{H}\boldsymbol{\Phi}, \tag{11}$$

where H denotes Hermitian (conjugate transpose) and where the vector of parameters $\hat{\boldsymbol{\delta}}$ and the data matrix $\boldsymbol{\Phi}$ are defined in (11).

$$\hat{\boldsymbol{\delta}} = \begin{bmatrix} \alpha_{oo} \\ \vdots \\ \alpha_{Po} \\ \vdots \\ \alpha_{oN} \\ \vdots \\ \alpha_{PN} \\ -\beta_{o1} \\ \vdots \\ -\beta_{P1} \\ \vdots \\ -\beta_{oD} \\ \vdots \\ -\beta_{PD} \end{bmatrix}, \quad \boldsymbol{\Phi} = \begin{bmatrix} x(k) \\ \vdots \\ x(k)|x(k)|^{P} \\ \vdots \\ x(k-\tau_N) \\ \vdots \\ x(k-\tau_N)|x(k-\tau_N)|^{P} \\ \hat{y}(k-\tau_1) \\ \vdots \\ \hat{y}(k-\tau_1)|\hat{y}(k-\tau_1)|^{P} \\ \vdots \\ \hat{y}(k-\tau_N) \\ \vdots \\ \hat{y}(k-\tau_N)|\hat{y}(k-\tau_N)|^{P} \end{bmatrix}. \tag{12}$$

In order to extract the vector of parameters $\hat{\boldsymbol{\delta}}$, we performed a least-squares (LS) identification from input–output (x_{PA}, y_{PA}) observations of the PA. The identification error is defined as

$$e(k) = y_{PA}(k) - \hat{y}(k), \tag{13}$$

and the LS solution for $\hat{\boldsymbol{\delta}}$ is therefore

$$\hat{\boldsymbol{\delta}} = (\boldsymbol{\Phi}^{H}\boldsymbol{\Phi})^{-1}\boldsymbol{\Phi}^{H}\mathbf{y}_{\mathbf{PA}}, \tag{14}$$

with $\mathbf{y_{PA}} = [y_{PA}(0), y_{PA}(1), \ldots, y_{PA}(L)\ ]^{\mathrm{T}}$ being the vector of output observations of length L.

The normalized mean square error achieved using the NARMA model, just considering one delayed sample of the input and another delayed sample of the output in the NARMA structure (small influence of memory effects), was about -43 dB.

V. DIGITAL PREDISTORTION LINEARIZATION

Figure 9 presents a block diagram of the digital baseband predistortion scheme that was adopted. To derive the predistortion function from the original NARMA behavioral model, it is necessary to rewrite the equations to obtain $x_A(k)$ in terms of the desired linear output $y_D(k)$. A detailed explanation on this procedure can be found in [13].

To implement the DPD in an FPGA, it is necessary to express the predistortion function as a combination of fundamental building blocks called BPCs. A BPC requires simple hardware blocks: a complex multiplier, a dual port RAM memory block acting as a LUT, an address calculator, and two ports of control. Further details on the implementation in an FPGA device can be found in [14]. The structure of the predistortion function, in terms of BPCs, is depicted in Fig. 10.

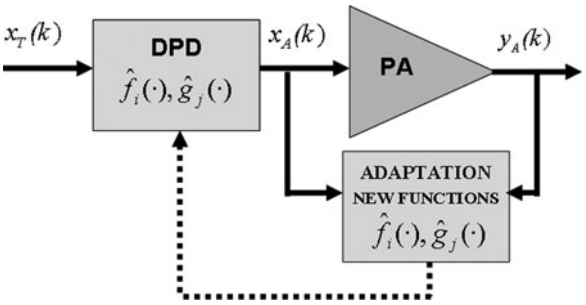

Fig. 9. Predistortion block diagram.

The predistortion function can be expressed in terms of combinations of BPCs as

$$x_A(k) = z(k)G_{\mathrm{LUT}\hat{f}_o^{-1}}(|z(k)|), \tag{15}$$

where $z(k)$ is defined as

$$z(k) = y_D(k) + \sum_{j=1}^{D} \underbrace{y_D(k-\tau_j)G_{\mathrm{LUT}}\hat{g}_j(|y_D(k-\tau_j)|)}_{\hat{g}_j(y_D(k-\tau_j))} - \sum_{i=1}^{N} \underbrace{x_A(k-\tau_i)G_{\mathrm{LUT}\hat{f}_i}(|x_A(k-\tau_i)|)}_{\hat{f}_i(x_A(k-\tau_i))}, \tag{16}$$

where G_{LUT} (for both $\hat{g}_j$ and $\hat{f}_i$) are complex gains stored in their corresponding LUT, $x_A(k)$ is the output of the DPD, and $y_D(k)$ is the desired output defined as the signal to be transmitted ($x_T(k)$) multiplied by a linear amplification (G_{linear}),

$$y_D(k) = x_T(k)G_{\mathrm{linear}}. \tag{17}$$

Then, the adaptive process followed by the digital adaptive DPD in order to perform the PA linearization consists in the following four steps: (1) to identify new nonlinear functions $\hat{f}_i$ and $\hat{g}_j$ by monitoring current PA input and output samples, (2) to test the stability of both PA and DPD NARMA models using the method proposed in [10], (3) to invert the nonlinear function $\hat{f}_o$ to find the DPD output, and (4) to generate all necessary LUT contents to implement the predistorter function; and then back to step 1. The identification of the PA behavioral model is performed obtaining the LS solution presented in (14). For this particular implementation, the LS takes complex data buffers of 2048 samples and a forgetting factor is adopted in order to prevent abrupt changes in the parameters that define the PA model.

In the case of the designed PA, good results were obtained with a predistorter function having only three BPCs to compensate for the nonlinear distortion and memory effects: in particular: the static BPC (associated to

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

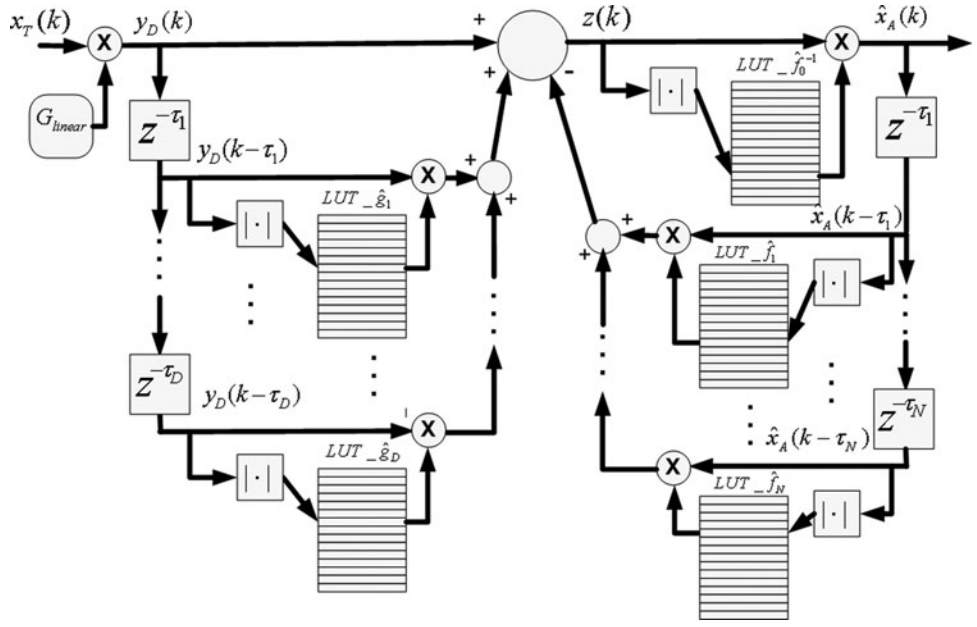

Fig. 10. Predistortion function.

f_0^{-1}), one BPC-FIR (associated to g_1), and one BPC-IIR (associated to f_1).

VI. VALIDATION RESULTS

In a first approach toward a final implementation, it is necessary to analyze the linearization capabilities shown by this NARMA-based DPD. The DPD linearizer has to be capable of compensating both in-band and out-of-band nonlinear distortion. To validate the functioning of the adaptive predistorter, an FPGA DPD simulator has been implemented in Matlab. This simulator emulates the DPD function as it is performed in an FPGA, that is, by means of a set of BPCs. Moreover, a NARMA behavioral model has been used to reproduce the nonlinear dynamics of the designed PA operating at 38 GHz. Both single carrier (SC) and OFDM 16-QAM test signals (roll-off = 0.22) presenting PAPRs around 9–10 dB have been considered.

To ensure a fair comparison, it is necessary to take into account unlinearized backed-off signals presenting similar mean output power to the linearized output signal. Figure 11 shows the AM–AM characteristics for: unlinearized PA, unlinearized PA with backoff operation, inverse PA characteristic, and the linearized PA. It is possible to observe that the DPD is capable of counteracting nonlinear distortion and get into compression in a linear way. Moreover, Fig. 12 and Fig. 14 shows the in-band distortion compensation achieved by the DPD, measured in terms of EVM. The 16-QAM constellation of the backed-off signal presents an EVM of around 11% (SC) and 37% (OFDM), respectively, while thanks to predistortion linearization it can be reduced up to less than 1%.

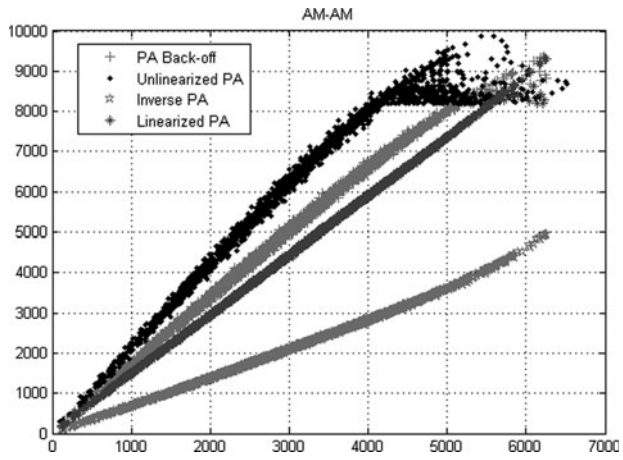

Fig. 11. PA AM–AM characteristics: unlinearized PA, unlinearized PA with back-off operation, inverse PA characteristic, and linearized PA.

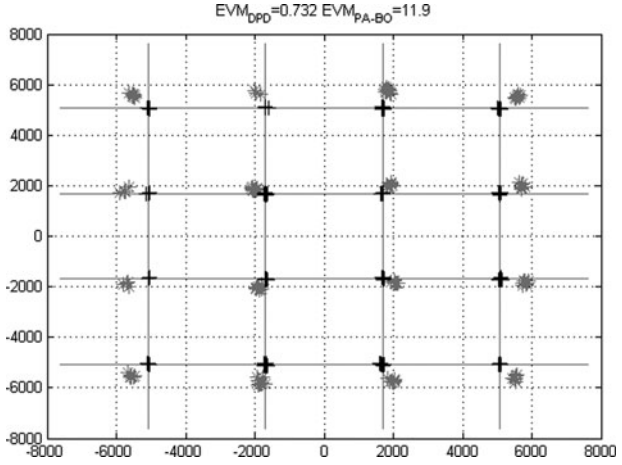

Fig. 12. SC 16-QAM constellation for both linearized (black) and backed-off output signals (gray).

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

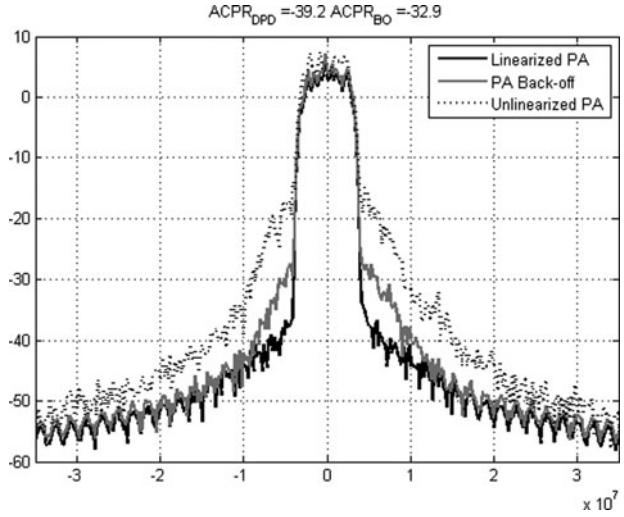

Fig. 13. Output power spectra (SC 16-QAM) for linearized PA, unlinearized PA, and unlinearized PA with back-off operation.

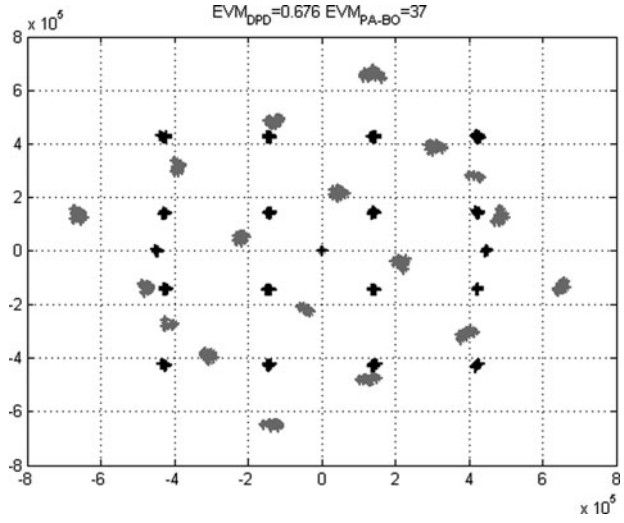

Fig. 14. OFDM 16-QAM constellation for both linearized (black) and backed-off output signals (gray).

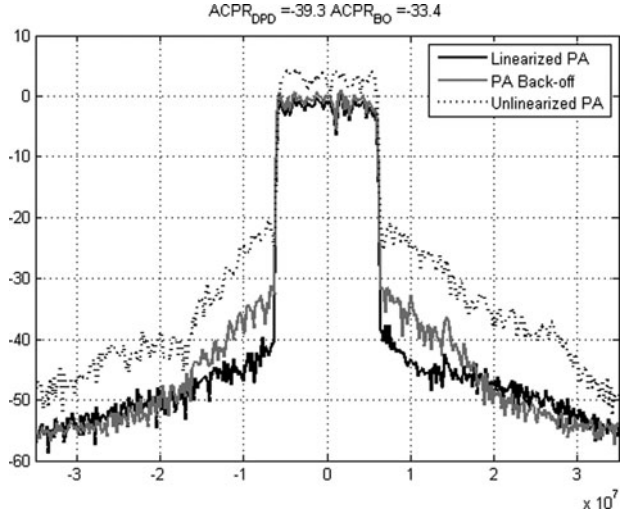

Fig. 15. Output power spectra (OFDM 16-QAM) for linearized PA, unlinearized PA, and unlinearized PA with back-off operation.

Finally, Figs 13 and 15 show the spectral regrowth reduction (out-of-band distortion compensation) of ∼6 dB achieved by the DPD in comparison to an unlinearized backed-off signal for both SC and OFDM configurations (Figs 13, 15).

VII. CONCLUSION

This paper has addressed the linearization of an mm-wave PA by means of an adaptive digital predistorter operating at baseband. This DPD is based in a NARMA structure that has been used for both characterizing and compensating PA nonlinearities and memory effects. Simulation results have evidenced that by means of the adaptive DPD it is possible to counteract the PA nonlinear behavior and thus to compensate both in-band and out-of-band distortion.

ACKNOWLEDGEMENT

This work was partly supported by the former EU network TARGET (IST-1–507893-NOE), by the Italian Ministry of University and Research (MIUR), and by the Spanish Government under project TEC2005-07985-C03–02.

REFERENCES

[1] Liu, T.; Boumaiza, S.; Ghannouchi, F.M.: Augmented Hammerstein predistorter for linearization of broad-band wireless transmitters. IEEE Trans. Microwave Theory Tech., **54** (2006), 1340–1349.

[2] Zhi-yong, H.; Jian-hua, G.; Shu-jian, G.; Gang, W.: An improved look-up table predistortion technique for HPA with memory effects in OFDM systems. IEEE Trans. Broadcasting, **52** (2006), 87–91.

[3] Melczarsky, I.; Gilabert, P.L.; Montoro, G.; Bertran, E.; Di Giacomo, V.; Filicori, F.: Behavioral modeling and digital predistortion for the linearization of a mm-wave power amplifier. TARGET Days 07 Rome, December 07, 41–46.

[4] Kenington, P.B.: High-Linearity RF Amplifier Design. Artech House Publishers, Boston, 2000.

[5] Santarelli, A. et al.: A simple non-quasi-static non-linear model of electron devices, in GAAS Symp. Paris, October 05, 305–308.

[6] Filicori, F.; Vannini, G.; Santarelli, A.; Mediavilla, A.; Tazon, A.; Newport, Y.: Empirical modeling of low-frequency dispersive effects due to traps and thermal phenomena in III-V FETs. IEEE Trans. Microwave Theory Tech., **43** (1995), 2972–2981.

[7] Mirri, D.; Iuculano, G.; Filicori, F.; Pasini, G.; Vannini, G.; Pellegrini, G.: A modified Volterra series approach for nonlinear dynamic system modeling. IEEE Trans. Circuits Syst. I, **49** (2002), 1118–1128.

[8] Vuolevi, J.: Distortion in RF Power Amplifiers. Artech House Publishers, Boston, 2003.

[9] Pedro, J.C.; Maas, S.A.: A comparative overview of microwave and wireless power-amplifier behavioral modeling approaches. IEEE Trans. Microwave Theory Tech., **53** (2005), 1150–1163.

[10] Gilabert, P.L.; Montoro, G.; Cesari, A.: A recursive digital predistorter for linearizing RF power amplifiers with memory effects, in Asia-Pacific Microwave Conf. Yokohama, December 06, 1043–1047.

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press

[11] Gilabert, P.L.; Silveira, D.; Montoro, G.; Gadringer, M.E.; Bertran, E.: Heuristic algorithms for power amplifier behavioral modeling. IEEE Microwave Wireless Compon. Lett., **17** (2007), 715–717.

[12] Gilabert, P.L.; Montoro, G.; Cesari, A.: A recursive digital predistorter for linearizing RF power amplifiers with memory effects, in Asia-Pacific Microwave Conf. Yokohama, December 06, 1043–1047.

[13] Montoro, G.; Gilabert, P.L.; Bertran, E.; Cesari, A.; Silveira, D.: A new digital predictive predistorter for behavioral power amplifier linearization. IEEE Microwave Wireless Compon. Lett., **17** (2007), 448–450.

[14] Gilabert, P.L.; Cesari, A.; Montoro, G.; Bertran, E.; Dilhac, J.M.: Multi look-up table FPGA implementation of an adaptive digital predistorter for linearizing RF power amplifiers with memory effects. IEEE Tran. Microwave Theory Tech., **56** (2008), 372–384.

Ilan Melczarsky received an electronics engineering degree (cum laude) from the University of Mar del Plata, Buenos Aires, Argentina, in 2000, and a Ph.D. degree in electronics and computer science from the University of Bologna, Italy, in 2005.

From 2000 to 2001, he has been a Senior Product Engineer with Ericsson Argentina. From 2002 to 2005, he was a Research Fellow with the Italian Research Council (CNR). Since 2005, he has been with the Dipartimento di Ingegneria Elettronica (DEIS), University of Bologna, as a Post-Doctoral Researcher and Teaching Assistant. His research interests include nonlinear characterization and modeling of high-frequency electron devices and circuits, electronic measurements, and high-frequency circuit design.

Pere Ll. Gilabert Pinal was born in Vilanova i la Geltrú, Barcelona (Spain) in 1978. He received the degree in telecommunication engineering from the Technical University of Catalonia (UPC) in 2002, and he developed his master's thesis at the University of Rome "La Sapienza" with an exchange grant. He joined the Department of Signal Theory and Communications (TSC) in 2003 and received his Ph.D. from the UPC in February 2008. His research is focused on system level linearization techniques for RF power amplifiers. Other research interests include digital signal processing for communications, communication electronics, and circuit theory. He is currently lecturing on undergraduate courses at the Castelldefels School of Technology (EPSC) as Assistant Professor.

Valeria Di Giacomo was born in Salerno, Italy. She received the Laurea degree in electronic engineering from the University of Bologna, Italy, in 2005.

Since then, she has collaborated with the Department of Electronics of the same University, and in 2006 she joined the Engineering Department of the University of Ferrara as a Ph.D. student. Her research activity is mainly oriented to nonlinear electron device modeling for microwave applications.

Eduard Bertran received the Engineer (option communication electronics) and Doctor Engineer degrees in telecommunication engineering, both from the Universitat Politècnica de Catalunya (UPC), Barcelona, Spain, in 1979 and 1985, respectively. He joined the Department of Signal Theory and Communications (TSC) in 1987, where he is currently a full professor. He has been the head of studies of the TSC department and an Associate Dean in different telecommunications schools. His research interests include control, communication electronics, signal processing, and circuit theory, topics where he has produced different books and peer-reviewed journal and conference papers. He is a member of IFAC and a senior member of IEEE. He has collaborated in different national and European research projects and teams.

Fabio Filicori received the Dr. Ing. degree in electronic engineering in 1974 from the University of Bologna, where he joined the Faculty of Engineering as Assistant Researcher and, later, as Associate Professor. In 1990 he became Full Professor of Electronics at the University of Perugia. In 1991 he moved to the University of Ferrara, where he was coordinator of the degree course in electronic engineering. Currently, he is Full Professor at the University of Bologna, where he has been coordinator of the Ph.D. course in electronics, computer science, and telecommunications. He has been the coordinator of research projects in electronic engineering promoted by the Ministry of University and Research. In 2007 he was appointed as member of the Technology Commission of the Italian Space Agency. He has been workpackage leader for the European NoE TARGET. He has been TPC chairman for the EUMIC Conference and editorial board member for IEEE MTT Transactions. He is the author of about 200 papers concerning his research in nonlinear microwave circuit design, electron device modeling, electronic measurements, and industrial electronics.

https://doi.org/10.1017/S1759078709000075 Published online by Cambridge University Press