International Journal of Microwave and Wireless Technologies, 2012, 4(5), 505–514.
doi:10.1017/S1759078712000517

RESEARCH PAPER

A high-speed buck converter for efficiency enhancement of W-CDMA power amplifiers

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We present a design strategy for a buck converter, which fulfills the high dynamic requirements of efficient envelope amplifier needed by modern efficiency enhancement techniques for power amplifiers*. The proposed DC–DC converter has an innovative control system, which makes it fast, robust, and resource saving. A mathematical model describes its dynamic behavior and is used to find a setup, which gives an optimal compromise between the dynamic performance and efficiency. The approach is applicable to various state-of-the-art communication standards. As an example, an envelope following (EF) power amplifier (PA) for the wideband code-division-multiple-access (W-CDMA) modulation scheme is treated. The corresponding buck converter is implemented in a monolithic chip (except the inductor and the capacitor of the output filter). The measurements with an industry standard W-CDMA PA (RMPA2265) match very well with the forecast of the model and confirm doubling of the average efficiency.*

Keywords: Circuit design and applications, Power amplifiers and linearizers

Received 2 January 2012; Revised 8 May 2012

I INTRODUCTION

Modern modulation schemes like wideband code-division multiple access (W-CDMA) have very high requirements concerning the linearity of the power amplifier (PA). Therefore, a variety of efficient PA architectures, for example, class B–F cannot be used due to their nonlinearities. The major drawback of the remaining architectures (classes A and AB) is a very poor efficiency if they operate in back-off. Because of the advanced output power regulation of state-of-the-art communication systems the back-off operation is very likely. Hence, the average efficiency of the PA is very low, which leads to a high-power consumption. This behavior shortens battery operation of the device and therefore limits the mobility of the user.

Several publications demonstrate different approaches to overcome this problem. There are hybrid amplifier configurations like Doherty amplifiers [1] and linear amplification with nonlinear components (LINC) [2]. But the on-chip realization of the required power divider and combiner is difficult and very lossy. A class of systems, which is much more attractive for a system-on-chip solution, modulates the supply voltage of the PA. The Kahn envelope elimination and restoration (EER) [3] technique divides the amplifier input signal in a magnitude and a phase branch. The phase is amplified with a high efficient but nonlinear PA. The envelope of the output signal is adjusted by a DC–DC converter, which is controlled by the magnitude branch and modulates the PA supply voltage. A similar approach creates the magnitude and phase information, which is already in the digital base band and is called polar transmitter [4]. The envelope following (EF) [4, 5] and envelope tracking (ET) [4, 6] techniques use linear PAs in class A or AB configuration. By modulating the supply voltage, the amplifier always operates very close to saturation. Thereby, its efficiency significantly increases. Whereas ET only follows slow changes of the input signal envelope caused by changing radio signal propagation conditions, *EF* also enables fast changes through the modulation.

All these techniques, except ET, have one thing in common: they need an efficient DC–DC converter with a very high bandwidth to follow the fast changing envelope signal. Hence, this work presents a systematic way to handle this challenge. Thereto, an accurate system model has to be developed. It is used to find the optimal configuration of the proposed buck converter. To prove the correctness and the feasibility of the theoretical part, a fully integrated (except for the capacitor and the inductance of the output filter) Complementary Metal Oxide Semiconductor (CMOS) circuit is presented. The measurements, taken on the buck converter and its application in an *EF* system with a W-CDMA PA, verify the performance of the design and the theoretical considerations.

II SYSTEM CONSIDERATIONS

The basis of the following analysis is the *EF* system depicted in Fig. 1. A buck converter, controlled by the envelope of the W-CDMA modulated RF input signal, is used to modulate the supply voltage of a PA in class A or AB configuration.

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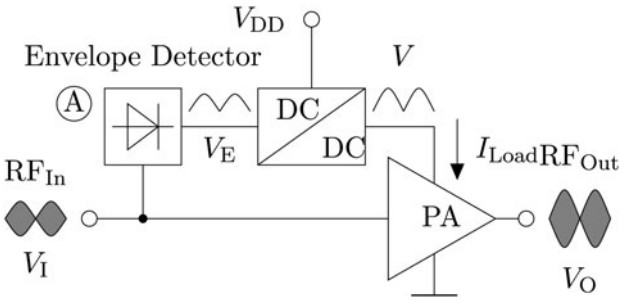

Fig. 1. Simplified diagram of linear power amplifier (PA) combined with the envelope following (EF) technique.

A) Buck converter

The majority of designs uses a pulse-width modulation (PWM) generator in conjunction with a proportional–integral–derivative (PID) controller to control the converter power switches [7, 8]. The behavior of this approach can be easily characterized by the means of linear control theory. The switching frequency is defined exactly through the fixed period of the PWM signal. But an implementation with a very high bandwidth is difficult due to the complexity of the individual components. Hence, the straightforward and robust sliding mode like control approach shown in Fig. 2 is applied. Its dynamic behavior is characterized by the following nonlinear delayed differential equation (DDE):

$$\dot{x}(t) = \begin{cases} A_- x(t) + b_- & \text{for } V_S(t-\Delta t) + \dfrac{\tau I_L}{C} < c^T x(t-\Delta t), \\ A_+ x(t) + b_+ & \text{otherwise.} \end{cases} \tag{1}$$

The vector $x = \begin{pmatrix} V & I \end{pmatrix}^T$ denotes the state of the system and consists of the voltage across the capacitor C and the current through the inductor L. The matrices $A_{-,+}$ and the vectors $b_{+,-}$ and c were introduced to present the DDE and also the following equations in a compact form. They are defined as follows:

$$A_{-,+} = \begin{pmatrix} -\dfrac{1}{CR_L} & \dfrac{1}{C} \\ -\dfrac{1}{L} & -\dfrac{R_{-,+}}{L} \end{pmatrix}, \quad b_- = \begin{pmatrix} -\dfrac{I_L}{C} & 0 \end{pmatrix}^T, \tag{2}$$
$$b_+ = \begin{pmatrix} -\dfrac{I_L}{C} & \dfrac{V_{DD}}{L} \end{pmatrix}^T, \quad c = \begin{pmatrix} 1 - \dfrac{\tau}{CR_L} & \dfrac{\tau}{C} \end{pmatrix}^T.$$

For a fixed setting of the power switches S an inhomogeneous differential equation describes the propagation of the state vector x. Hence, it is possible to introduce an affine transformation

$$\mathcal{T}^{\sigma}_{\Delta t} x = e^{A_\sigma \Delta t}(x(t) - x_\sigma) + x_\sigma = x(t + \Delta t), \quad \sigma \in \{-, +\}, \tag{3}$$

which evaluates the propagation of the space of all state vectors (phase space) for a given time t and the setting σ of S. As A_σ is a 2×2 matrix, the exponential matrix used in this equation can be calculated in the following way:

$$e^{A_\sigma t} = e^{-\delta_\sigma t}\left[1 \cos\ \Omega_\sigma t + \frac{A_\sigma + 1\delta_\sigma}{\Omega_\sigma} \sin\ \Omega_\sigma t\right]. \tag{4}$$

The variable δ_σ denotes the real part and Ω_σ the positive imaginary part of the two conjugate complex eigenvalues of A_σ

$$\delta_\sigma = \frac{1}{2CR_L} + \frac{R_\sigma}{2L}, \quad \Omega_\sigma = \sqrt{\frac{1}{LC}\left(1 + \frac{R_\sigma}{R_L}\right) - \delta_\sigma^2}. \tag{5}$$

The stationary state for each setting of the power switches is characterized by the vectors

$$x_- = \frac{1}{R_L + R_-}\begin{pmatrix} -I_L R_- R_L \\ I_L R_L \end{pmatrix}, \tag{6}$$

$$x_+ = \frac{1}{R_L + R_+}\begin{pmatrix} [V_{DD} - I_L R_+] R_L \\ V_{DD} + I_L R_L \end{pmatrix}. \tag{7}$$

Assuming that the input signal V_S is continuous, the points in time t_K when S are changing their state are specified by the following transcendental nonlinear system of two equations:

$$\begin{aligned} V_S(t_{2k+1} - \Delta t) + \frac{\tau I_L}{C} &= c^T \mathcal{T}^{-}_{\Delta t_{2k} - \Delta t} x_{2k}, \\ V_S(t_{2k+2} - \Delta t) + \frac{\tau I_L}{C} &= c^T \mathcal{T}^{+}_{\Delta t_{2k+1} - \Delta t} x_{2k+1}, \\ \text{with } \Delta t_k = t_{k+1} - t_k \text{ and } x_k &= x(t_k). \end{aligned} \tag{8}$$

If there exists more than one solution for t_{2k} or t_{2k+1}, the smallest positive one has to be used for further considerations. With the set of n points in time t_k and an initial condition $x(t_o)$ the state of the model is determined for all times $t_o < t$

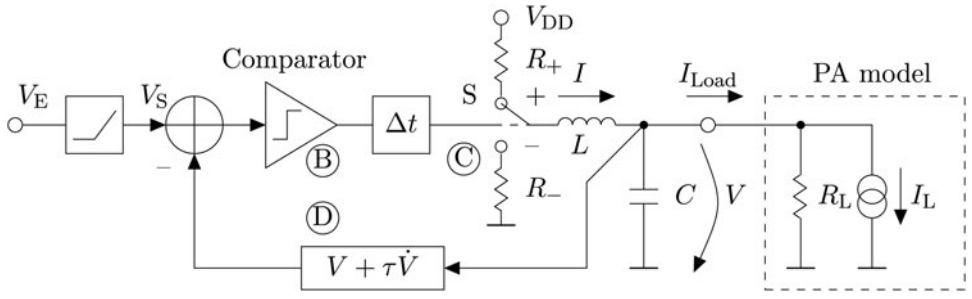

Fig. 2. Model of the proposed buck converter control architecture.

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$< t_n$ by a recursive equation as follows:

$$x(t) = \begin{cases} \mathcal{T}^{-}_{t-t_{2k}} x_{2k} & \text{for } t_{2k} \le t \le t_{2k+1}, \\ \mathcal{T}^{+}_{t-t_{2k+1}} x_{2k+1} & \text{for } t_{2k+1} < t < t_{2k+2}. \end{cases} \quad (9)$$

The system (8) is well suited for numerical evaluation but it does not have an analytical solution. To overcome this problem it is linearized. This leads to the following analytical approximations for the points in time when S changes its state:

$$t_{2k+1} = \frac{c^T\left(\mathcal{T}^{+}_{-\Delta t} - \mathcal{T}^{-}_{-\Delta t}\right)x_{2k}}{c^T e^{-A_- \Delta t}(A_- x_{2k} + b_-) - \dot{V}_{S2k}} + t_{2k}, \quad (10)$$

$$t_{2k+2} = \frac{c^T\left(\mathcal{T}^{+}_{-\Delta t} - \mathcal{T}^{-}_{-\Delta t}\right)x_{2k+1}}{-c^T e^{-A_+ \Delta t}\left(A_+ x_{2k+1} + b_+\right) + \dot{V}_{S2k}} + t_{2k+1}. \quad (11)$$

Now, two important parameters of the buck converter, the switching frequency

$$f_{2k} = \frac{1}{t_{2k+2} - t_{2k}} \quad (12)$$

and the duty cycle

$$d_{2k} = \left(t_{2k+2} - t_{2k+1}\right) f_{2k} \quad (13)$$

at the output of the power switches can be calculated. Ideally, the output voltage V of the DC–DC converter follows exactly the control signal V_E of the envelope detector. Due to the delay Δt of the comparator such behavior is impossible. The best case, which can be achieved, is described by the following equation:

$$V_{2k+2} = V_{E2k} + \frac{\dot{V}_{E2k}}{f_{2k}} \text{ with } V_{E/Sk} = V_{E/S}(t_k - \Delta t). \quad (14)$$

A linear approximation of the output voltage propagation at the duty cycle d allows the matching between the present and the desired behavior,

$$V_{2k+2} = e_V^T \mathcal{T}^{+}_{\Delta t_{2k+1}} \mathcal{T}^{-}_{\Delta t_{2k}} x_{2k} \qquad \text{with } e_V^T = \begin{pmatrix} 1 & 0 \end{pmatrix} \quad (15)$$

$$= V_{2k} + \frac{V_{2k} + \alpha_d V_{S2k} + \gamma_d + \mathcal{O}(d_{2k} - d)}{\beta_d f_{2k}}. \quad (16)$$

The method of equating coefficients applied on the last two equations results in the function

$$V_S = \alpha_d V_E + \beta_d \dot{V}_E + \gamma_d \quad (17)$$

which can be used to correct the dynamic behavior of the proposed buck converter. Its coefficients α_d, β_d, and γ_d are calculated as follows:

$$\beta_d = \left(\sum_\sigma W_\sigma(d) \frac{\Delta t \tau_\sigma \exp -\delta_\sigma \Delta t}{(\tau - \tau_\sigma)\text{sinc}\ \Omega_\sigma \Delta t}\right)^{-1} \quad (18)$$

with $\text{sinc} = \dfrac{\sin(x)}{x}$

$$\alpha_d = \beta_d \sum_\sigma W_\sigma(d) \frac{1 - 2\delta_\sigma \tau_\sigma + \left(\dfrac{R_\sigma}{R_L} + 1\right)\omega_0^2 \tau \tau_\sigma}{\tau - \tau_\sigma}, \quad (19)$$

$$\gamma_d = \frac{I_L}{C}\left(\beta_d - \tau\right) - e_V^T\left(\alpha_d E + \beta_d A\right) \sum_\sigma W_\sigma(d) \mathcal{T}^{\sigma}_{\Delta t} 0 \quad (20)$$

$$\text{with} \quad W_\sigma(d) = \begin{cases} d & \text{for } \sigma = -, \\ 1 - d & \text{for } \sigma = +. \end{cases}$$

The function $\beta_d(\tau)$ has two simple zeros at τ_- and τ_+, which are given by the following equation:

$$\tau_\sigma = \frac{1}{\Omega_\sigma \cot\ \Omega_\sigma \Delta t + \delta_\sigma}. \quad (21)$$

These zeros have a major influence on the stability of the proposed control approach. The system becomes instable if

$$\tau \le \max\ \left\{\tau_+, \tau_-\right\} = \tau_{Crit}. \quad (22)$$

With the help of (17) the desired behavior (14) is only achieved, if the linear approximation is valid. As significant evidence the time differences $t_{\Delta 2k}$ and $t_{\Delta 2k+1}$ have to be positive. This condition results in two inequalities

$$\dot{V}_{S2k} > c^T e^{-A_- \Delta t}(A_- x_{2k} + b_-), \quad (23)$$

$$\dot{V}_{S2k} < c^T e^{-A_+ \Delta t}\left(A_+ x_{2k+1} + b_+\right). \quad (24)$$

One major goal during the design of the buck converter is to ensure their compliance for nearly all states of operation.

The energy loss in the power switches of the DC–DC converter during the time t with the initial state x and the switch state σ is denoted by

$$\mathcal{L}_t^\sigma x = R_\sigma \int_0^t \left(\mathcal{T}_{t'}^\sigma x\right)^T \begin{pmatrix} 0 & 0 \\ 0 & 1 \end{pmatrix} \mathcal{T}_{t'}^\sigma x \, dt'. \quad (25)$$

The used output energy is described in the same way

$$\mathcal{U}_t^\sigma x = \int_0^t \left[\left(\mathcal{T}_{t'}^\sigma x\right)^T \frac{1}{R_L} \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix} \mathcal{T}_{t'}^\sigma x + I_L \begin{pmatrix} 1 & 0 \end{pmatrix} \mathcal{T}_{t'}^\sigma x\right] dt'. \quad (26)$$

The lost/used power of the buck converter during one switch cycle (time interval $[t_{2k+2}, t_{2k}]$) is calculated as follows:

$$P_L(x_{2k}) = \left(\mathcal{L}^{+}_{\Delta t_{2k+1}} x_{2k+1} + \mathcal{L}^{-}_{\Delta t_{2k}} x_{2k} + E_{SW}\right) f_{2k}, \quad (27)$$

$$P_U(x_{2k}) = \left(\mathcal{U}^{+}_{\Delta t_{2k+1}} x_{2k+1} + \mathcal{U}^{-}_{\Delta t_{2k}} x_{2k}\right) f_{2k}. \quad (28)$$

The constant E_{SW} denotes the dynamic energy loss in the power switches during this switch cycle.

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B) Statistical description of the envelope

The envelope of the PA RF input signal changes on two time scales: the first one is caused by the modulation and the second one by the power control of the mobile terminal. Both have to be taken into account to get an accurate description of the statistical properties of the envelope signal, which is proportional to the input voltage V_E of the buck converter. For the sake of a compact description the envelope signal is normalized

$$h(t) = \frac{\hat{V}_I(t)}{\sqrt{2R_0\bar{P}_I}}, \qquad \bar{P}_{I/O} = \frac{1}{R_0 T_P}\int_{t_0}^{t_0+T_P} V_{I/O}^2(t)\,dt. \quad (29)$$

The constant R_0 denotes the input resistance of the PA and T_P is the typical time between the change of the output power through the power control.

The hybrid phase shift keying (HPSK) modulation [9] used by W-CDMA causes fast changes in the envelope h. The statistic properties of h are derived from simulation results of a HPSK modulator implemented in MATLAB®. This method is preferred over an analytic model because of the high complexity of the modulation scheme. The simulation uses the 768 kb/s uplink reference measurement setup, which is given by the 3rd generation partnership project (3GPP) [10], and uniform distributed random input data. The probability density function (pdf) $p_F(h, \dot{h}, \ddot{h})$ represents the fast changes caused by the modulation and results from the analysis of 3.84×10^5 chips with 16 samples per chip. Its isosurface $p_F = 1$ is depicted in Fig. 4. The shape in the middle of the diagram, which looks like a spinning, represents smooth changes in the envelope. The two arcs are caused by large and fast changes of h. The power control of a mobile terminal adapts the RF output power $\bar{P}_O$ to the radio signal propagation conditions. Figure 3 depicts the pdf $p_S(\bar{P}_O)$, which demonstrates that the PA rarely operates at its maximum output power $\bar{P}_{Om}$. The following equation combines p_F and p_S:

$$p_M(h, \dot{h}, \ddot{h}) = \int_0^{\bar{P}_{Om}} p_s(\bar{P}_o)\,p_F\left(\xi h, \xi\dot{h}, \xi\ddot{h}\right) d\bar{P}_o \quad (30)$$

$$\text{with } \xi(\bar{P}_O) = \sqrt{\frac{\bar{P}_O}{\bar{P}_{Om}}}.$$

Now, all the statistic properties of h, needed for the optimization of the design, are characterized.

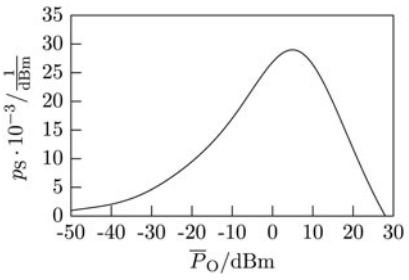

Fig. 3. The probability density function of the PA RF output power [6] for W-CDMA.

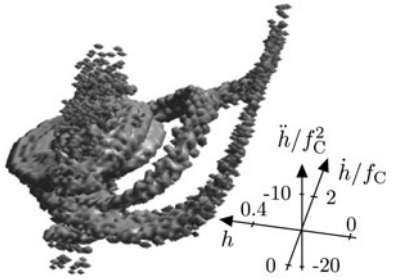

Fig. 4. Isosurface ($p_F = 1$) which reflects the fluctuation of the envelope h due to modulation. The variable f_C denotes the W-CMDA chip rate of 3.84 MHz.

C) Optimization of the design parameter

Altogether five parameters (Δt, L, C, τ, and V_{DD}) and the dimension of the power switches completely describe the modeled buck converter. To find their optimal values, first of all the switching frequency f_S of the DC–DC converter has to be specified. To achieve a low ripple on the PA supply voltage, this value should be much higher than the corner frequency of the output low-pass filter (formed by the inductor L and the capacitor C). On the other hand, the efficiency of the buck converter decreases with rising switching frequency, is due to the dynamic losses in the power switches, which are proportional to f_S. Additionally, the available semiconductor technology limits the switching frequency. In contrast to a PWM controlled buck converter, f_S of the proposed design is not constant, but a function of the circuit input signal. Hence, the maximum switching frequency f_{SM}, which can be approximated by the following rule of thumb (assuming that $A_- \approx A_+ \approx A$ and $x_{2k} \approx x_{2k} + 1$):

$$f_{SM} = \max f_{2k} \overset{(12)}{\approx} \frac{c^T e^{-A\Delta t}\left(b_- - b_+\right)}{4c^T\left(e^{-A\Delta t} - 1\right)\left(x_+ - x_-\right)} \approx \frac{1}{4\Delta t} \quad (31)$$

will be taken into account. For the deployed IBM BiCMOS 7WL technology, a maximum switching frequency of 50 MHz provides an ideal trade-off between low output ripple and high efficiency. So according to (31) the delay of the control circuit Δt equals 5 ns.

In order to combine the results of the mathematical model and the statistic properties of the envelope the state x_{2k} of the buck converter has to be defined

$$x_{2k} = \begin{pmatrix} I_{2k} & V_E \end{pmatrix}^T$$
$$\text{with } I_{2k} = \frac{V_E}{R_L} - \frac{C}{\beta_0}\left[\left(\alpha_{0.5} - \alpha_0\right)V_E + \beta_{0.5}\dot{V}_E + \gamma_{0.5} - \gamma_0\right]. \quad (32)$$

The DC–DC converter is able to follow the envelope signal, as long as the series of t_k is monotonically increasing. This condition is fulfilled, if the denominators of (10) and (11) are both positive. The first equation describes the span of time during which the output voltage V is falling to the desired value. The linearity of the PA is not affected if the supply voltage decreases too slowly. Much more critical is such behavior during the rise of V, which is indicated by a negative denominator of (11). To avoid these operation states, the supply

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voltage has to fulfill the following relation:

$$V_{DD} > \frac{LC}{\beta_1}\left[c^T e^{-A_+\Delta t}\left(A_+ x_{2k+1} - \frac{I_L}{C} e_V^T\right) - \dot{V}_S\right] \quad (33)$$

$$= a_3 \ddot{V}_E + a_2 \dot{V}_E + a_1 V_E + a_0. \quad (34)$$

To achieve preferably small values of V_{DD}, the damping δ_+ should be minimal. So the requirement

$$C = \frac{L}{R_+ R_L} \quad (35)$$

reduces the dimension of the parameter space by one. The PA-dependent voltage V_H, V_o, and V_{Emin} establishes the connection between the input voltage of the buck converter V_E and the normalized envelope:

$$V_E = \begin{cases} V_{Emin}, & V_H h + V_o < V_{Emin}, \\ V_H h + V_o & \text{otherwise.} \end{cases} \quad (36)$$

The probability, that the supply voltage V_{DD} does not satisfy (33) during n of N switching cycles, is

$$P_V(V_{DD}) = \lim_{N\to\infty} \frac{n}{N} = 1 - \int_{-\infty}^{\infty} p_V(V_{DD})\, dV_{DD}. \quad (37)$$

Thereby, the probability density function p_V is derived from the envelope statistic in the following way:

$$p_V(V_{DD}) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} p_F\left(h^*, \dot{h}, \ddot{h}\right) d\dot{h}\, d\ddot{h}, \quad (38)$$

$$h^* = \frac{1}{a_1}\left[\frac{V_{DD} - a_o - a_1 V_o}{V_H} - a_2 \dot{h} - a_3 \ddot{h}\right]. \quad (39)$$

The coefficients a_o, a_1, a_2, and a_3, which are required to evaluate h^*, result from equating the corresponding coefficients of (33) and (34). The diagram in Fig. 5 shows P_V as a function of the output filter's corner frequency f_o for different supply voltages[1] It shows, that f_o and V_{DD} are interchangeable: the same dynamic behavior can be achieved with a low corner frequency and a high supply voltage and the other way around. To keep the output ripple of the buck converter low, the value of f_o should be at least five times lower than the maximum switching frequency f_{SM}. By setting $\tau = 20\tau_{Crit}$ the stability of the circuit is ensured. With respect to these requirements, the values, which are marked in Fig. 5 with a cross, were chosen for V_{DD} and f_o. The power switches are a chain of tapered CMOS inverters (tapering factor $\nu = 9$). So the transistors parameters can be derived from the parameters of the last inverter, which consists of p- and nMOSFETs. To minimize the parasitic capacitances and the channel resistance their length has been set to the technology minimum of 400 nm. Hence, the remaining parameters are the width of the p- (w_p) and the nMOSFET (w_n). The values of the model parameter R_+, R_- and E_{SW} are calculated by transient simulations for varying values of w_p and w_n. The mathematical

[1] All results shown in this section are based on the parameters of the RMPA2265 PA in low-power operation mode. $I_L = -19.6$ mA, $R_L = 10.5\ \Omega$, $V_o = 0.35$ V, $V_H = 1.13$ V and $V_{Emin} = 0.55$ V.

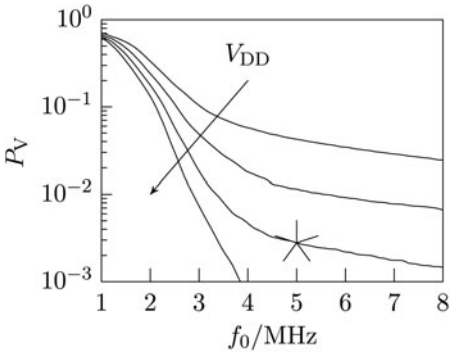

Fig. 5. The probability, that the DC–DC converter is not able to follow the envelope signal as a function of the supply voltage $V_{DD} = \{1.9\text{ V}, 1.95\text{ V}, 2\text{ V}, 2.05\text{ V}\}$ and the corner frequency f_o of the output filter.

model allows to calculate the loses P_L of the DC–DC converter and the DC power used by the PA P_U in the following way:

$$\bar{P}_{L/U}(w_p, w_n) = \int P_{L/U}(h, \dot{h}, \ddot{h}) p_M(h, \dot{h}, \ddot{h})\, dh\, d\dot{h}\, d\ddot{h}|_{w_p, w_n}, \quad (40)$$

where $P_{L/U}(h, \dot{h}, \ddot{h})$ is equivalent to $P_{L/U}(x_{2k})$ from (27) and (28), respectively, with x_{2k} according to (32) and (36). Out of these two quantities the efficiency of the buck converter can be determined easily by

$$\eta_B = \frac{\bar{P}_U}{\bar{P}_U + \bar{P}_L}. \quad (41)$$

Its value is depicted in Fig. 6 as a function of w_p and w_n. The cross marks the configuration, which was chosen for the design. It is a little bit displaced to the maximum, to avoid too large values of R_+ and R_-, which downgrade the P_V (V_{DD}). A summary of all design parameters is given in Table 1.

III CIRCUIT DESIGN AND IMPLEMENTATION

The complete chip consists of four building blocks, which are integrated into a monolithic chip and occupy an area of

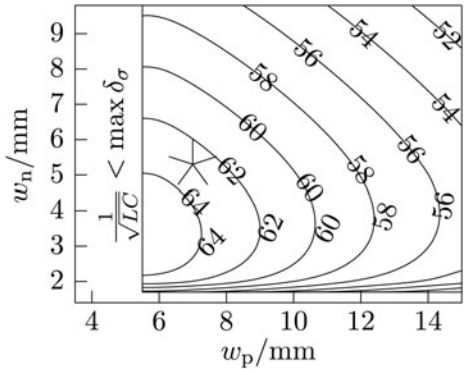

Fig. 6. Contour plot of the buck converter efficiency η_B versus the dimension of the power switches.

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Table 1. Summary of the optimized parameters.

Parameter	Designed	Measured
C	20 nF	–
L	50 nH	–
V_{DD}	2 V	–
Δt (ns)	5	(4.45 ± 0.1)
τ (ns)	90	109
R_+ (Ω)	1.23	1.33
R_- (Ω)	0.49	0.50
E_{SW} (nJ)	109	(177 ± 1)

0.54 mm². Their circuits and interconnections are depicted in Fig. 7. The dashed lines frame the different parts of the circuit, already known from the system model in Figs. 1 and 2. The starting point for the design of each block is the set of optimized parameters of the buck converter model, which is derived in the last section and summarized in Table 1.

A) Envelope detector

The circuit of this block is well known as diode detector. The block capacitor C_0 decouples the DC part of the RF input signal. Only the positive half-wave of the remaining signal passes the Schottky diode D1. An RC filter, which consists of R_1, R_2, C_1, and C_2 suppresses the carrier of the W-CDMA modulated RF signal and implements the derivation in (17). Its transfer function has a pole of order two at $f_1 = 15$ MHZ which is about four times higher than the chip rate of the W-CDMA signal and a simple zero at

$$f_2 = \frac{\alpha_{0.5}}{2\pi\beta_{0.5}} = \frac{\alpha_{0.5}}{2\pi R_2 C_2} = 2.31\,\text{MHz}. \tag{42}$$

Thus, a good carrier rejection is achieved, and simultaneously the distortion of the envelope signal is acceptable. The comparator uses current signals. Hence, a current mirror transfers the current through R_1 (output signal of the RC filter) to the envelope detector output current I_-. To avoid an input power dependent offset of this signal, a dummy diode detector is employed. The minimal output voltage of the buck converter V_o is adjusted by the external resistor R_3.

B) Comparator

The output current of the proportional differential feedback I_+ is inverted by a current mirror and fed to the input of a CMOS inverter (T1 and T2). Thus, the input current of the inverter is the difference ΔI between the I_+ and I_-, the output currents of the proportional differential feedback and the envelope detector. This small part of the whole block already shows the desired behavior: if ΔI is negative the inverter output switches to the supply voltage or else to ground. To increase the speed of the comparator a chain of multiple stages with low gain is preferred over one stage with a high gain [11]. Hence, the gain of the inverter is reduced by degeneration. For this purpose, T3 is operated in linear region to form a feedback resistor. Two adjacent common-source stages compensate the gain losses due to the degeneration. With the help of this technique a very low delay time of 1.9 ns is achieved. The output of the last source stage drives a chain of seven CMOS inverters. Three of them belong to the comparator. They ensure that the input signal of the power switches, formed by the remaining four inverters, is rail to rail.

C) Power switches

As already mentioned the power switches are formed by a chain of four tapered CMOS Inverters. They have a separate voltage supply to avoid interferences with the other blocks of the circuit. About 65% of the chip area (without pads) is occupied by them. Figure 6 shows the configuration of the power switches, which are an optimum trade-off between efficiency and speed. In this configuration the pMOSFET of the biggest inverter in the tapered chain has a width of $w_+ = 7100\,\mu$m and the corresponding nMOSFET has a width of $w_- = 5900\,\mu$m. The dimensions of the driver stages in the chain result from the tapering factor $\nu = 9$ and are listed in Table 2.

In conjunction with the comparator transient simulations show a total delay Δt of 4 ns. To compensate process variations, this value is consciously a little bit smaller than the one calculated in Section II(C).

D) Proportional differential feedback

To make the design more flexible, the feedback circuit processes an input signal range between zero and 1 V. In doing

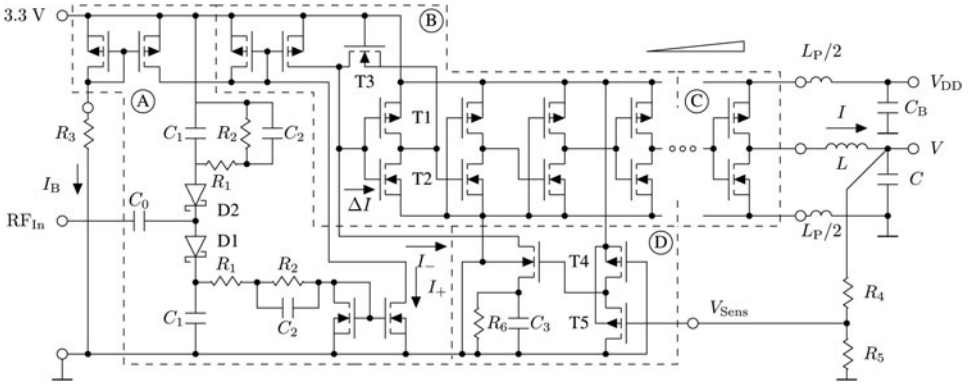

Fig. 7. Complete circuit of the designed buck converter.

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Table 2. Dimension of the driver stages of the power switches.

Stage	1 (μm)	2 (μm)	3 (μm)
Width pMOSFET	784	84	9.3
Width nMOSFET	700	80	8.9

so the ratio between the envelope of the RF input signal and the output voltage V is adjustable by an external voltage divider (R_4 and R_5). Although the PA parameter V_H can be fine tuned during the measurements. As the comparator requires a current signal, the input voltage is converted to the output current I_+ by a source follower. The capacitor C_3 in its load impedance induces the desired differentiating behavior

$$\tau = R_6 C_3 = 90\,\text{ns}. \tag{43}$$

A level shifter, which consists of T4 and T5, guarantees that the transistor of the adjacent source follower does not leave the saturation region over the complete input voltage range.

IV MEASUREMENTS

Because of the external capacitor and inductor, which form the output filter, measurements were performed on a PCB, which houses the chip (shown by Fig. 8a) and all external components. The major challenge of the PCB design is the total parasitic inductance L_P in the power switches voltage supply. Because they switch high currents up to 400 mA in very short periods of time (about 500 ps), even a small inductance causes large voltage spikes. Thereby in worst case the supply voltage of the power switches raises transiently beyond the breakdown voltage of the used CMOS transistors. To avoid such conditions there are three possibilities: The supply voltage, the parasitic inductance, or both of them have to be reduced. The diagram in Fig. 9 shows the maximum supply voltage V_{DD} (plotted over L_P), which guarantees that the breakdown voltage of 3.6 V is not exceeded. These results were obtained by a parametric transient simulation.

An external capacitor C_B with a value of 100 nF and an extreme low equivalent series inductance (ESL) of 200 pH decouple the fast changing currents form the rest of the PCB. So only the tracks and wires, which connect it to the chip, have to be taken into account. To keep them as small as possible, the capacitor is placed direct under the chip on the bottom side of the board. On account of the layout's symmetry, it is adequate to analyze only the upper half of these connections. They are depicted by Fig. 8a. The decoupling capacitor has eight terminals, four on each side. They connect alternating the two plates of the capacitor. Hence, the fast changing currents ΔI_{DD} in two adjoining tracks/bond wires are always in opposite directions. So the magnetic fields created by them, partly compensate each other. Thus, the parasitic inductances can be decreased significantly. The electromagnetic analysis software Sonnet® calculates a L_P of 943 pH for the described geometry. Hence, according to Fig. 9 the maximum supply voltage of the power switches (with a load of 400 mA) is 2.3 V. That is why the low-power mode of the PA (RMPA2265) is used. The high-power mode would need a supply voltage of 3.3 V.

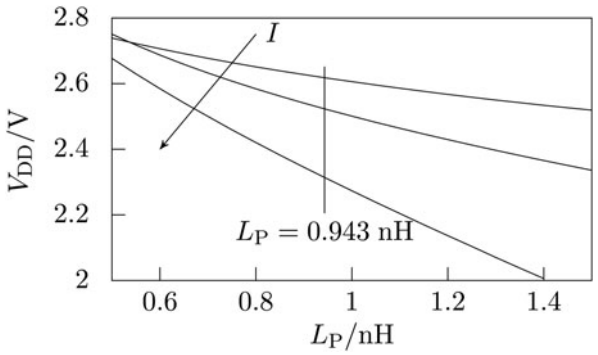

Fig. 9. The maximum supply voltage V_{DD} of the power switches as a function of the parasitic inductance L_P and the current $I = \{0, 200\,\text{mA}, 400\,\text{mA}\}$.

A) Model parameters of the buck converter

In order to quantify the resistances R_+ and R_- of the power switches, the input V_{Sens} of the chip is connected to an external voltage source. By increasing or rather decreasing its voltage, the state of the power switches can be toggle. A constant current source is applied to the output of the buck converter. For both states of the switches its current is swept from −200 to 200 mA. Through the measurement of the output voltage V two voltage–current characteristics arise. Each of them is

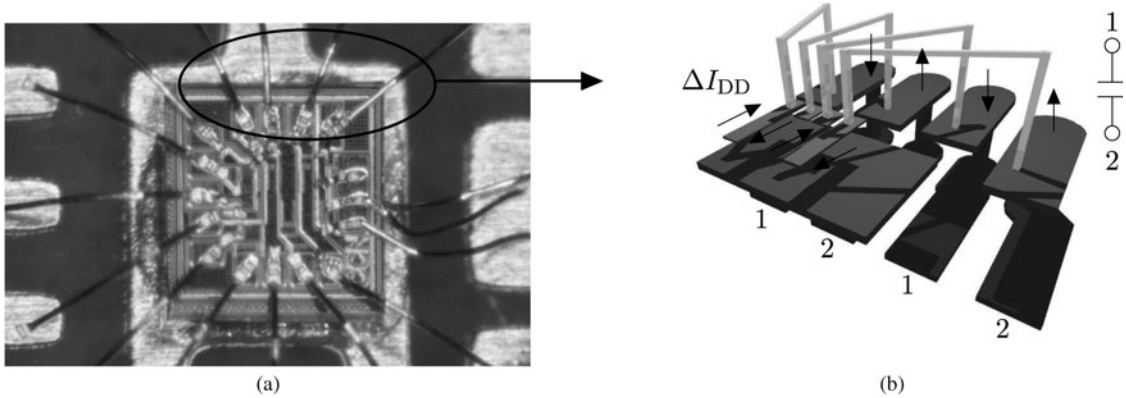

Fig. 8. Realization of the power switches voltage supply. (a) Photo of the fabricated chip (b) Model of the connection between the chip and the decoupling capacitor C_B (only the upper half is shown)

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approximated well by a linear function, whose slope is equal to the resistance in demand.

To find out the value of the time constant τ, the input V_{Sens} is connected to a sine wave generator. The amplitude and offset of this generator are chosen in a way, that the power switches can be fixed in both states (without any further switching cycles) by varying the bias current I_B. For different frequencies f of the sine wave I_B is adjusted, until the power switches stop changing their state and only the one, which connects the output of the chip to ground, is active. After a sweep over a frequency range from 100 to 10 MHz the amplitude of the generator is set to zero (its offset is maintained). The bias current is adjusted like before and its value is assigned to the variable I_{Bo}. The approximation of the measurements by the function

$$I_B(f) = I_{Bo} - K(1 + \tau 2\pi f), \tag{44}$$

results in the demanded time constant.

In an additional measurement, the buck converter is operated without a load ($I_L = 0$ and $R_L \to \infty$). Its output voltage V is set by means of an RF signal generator, which feeds an unmodulated 1.95 GHz carrier with the power $\bar{P}_I$ in the input of the envelope detector. The output of the power switches is connected to an oscilloscope. It is used to measure the period of time Δt_o during which the switch to the supply voltage is active and Δt_1 vice versa. Furthermore, the average current $\bar{I}_{DD}$ drained from the source V_{DD} is recorded. Because the input voltage V_E of the DC–DC converter remains constant during each measurement, its state x_o has to fulfill the following equation:

$$x_o = \mathcal{T}^+_{\Delta t_1} \mathcal{T}^-_{\Delta t_o} x_o. \tag{45}$$

So x_o and the corresponding state x_1 after the time Δt_o can be calculated as follows:

$$x_o = \left(E - e^{A_+ \Delta t_1} e^{A_- \Delta t_o}\right)^{-1} \mathcal{T}^+_{\Delta t_1} \mathcal{T}^-_{\Delta t_o} 0, \tag{46}$$

$$x_1 = \mathcal{T}^-_{\Delta t_o} x_o. \tag{47}$$

Due to $V_E = const.$ the equation

$$c^T \left(\mathcal{T}^+_{-\Delta t} x_o - \mathcal{T}^-_{-\Delta t} x_1\right) = 0 \tag{48}$$

is valid. It is used to obtain the value of Δt, because all other variables it contains are already known.

The dynamic losses of the power switches can also be derived from the measured data

$$P_{SW}(f_o) = E_{SW} f_o = V_{DD} \bar{I}_{DD} - \left(\mathcal{L}^-_{\Delta t_o} x_o + \mathcal{L}^+_{\Delta t_1} x_1\right) f_o. \tag{49}$$

With the help of this relation, E_{SW} can be calculated easily. To get more accurate results, the shown procedure is repeated for different output voltages V. Table 1 summarizes the measured parameters of the buck converter. The parameters specified during the design of the circuit and the measured ones match well.

B) Complete system

Now the designed circuit is used to modulate the supply voltage of a commercial standard W-CDMA PA (RMPA2265). Because this PA is a two-stage design, only its second and final stage is connected to the buck converter. Its first stage is supplied by a constant supply voltage and is neglected in the following considerations. The RMPA2265 is operated in the low-power mode, which has a linear output power of 16 dBm. Two properties have to be determined for the PA with a fixed supply voltage and the *EF* configuration: the efficiency and the linearity. The efficiency is defined as the ratio of the complete system power consumption and the output power of the PA. To compare both configurations the efficiency gain

$$G = \frac{\eta_{EF}}{\eta} \tag{50}$$

is introduced. In this equation, η_{EF} enotes the efficiency of the *EF* configuration and η describes the efficiency of the PA with a fixed supply voltage. As a measure for the linearity of the PA the adjacent channel leakage power ratio (ACLR) of its output signal is used. It is measured by a R&S® FSU 67 spectrum analyzer in the first and second, left and right adjacent channel. The W-CDMA modulated test signal[2], which feeds the PA, is generated by a R&S® SMBV100A vector signal generator. Figure 10 depicts the results of the measurements. It shows a significant efficiency gain at low output powers $\bar{P}_O$. The values of G can also be calculated with the mathematical model of the buck converter

$$G = \frac{\int \left(\frac{V_E(\xi h)}{R_L} - I_L\right) V_E(\xi h) p_F(h, \dot{h}, \ddot{h})\, dh\, d\dot{h}\, d\ddot{h}}{\int \left(P_U(\xi h, \xi \dot{h}, \xi \ddot{h}) + P_L(\xi h, \xi \dot{h}, \xi \ddot{h})\right) p_F(h, \dot{h}, \ddot{h})\, dh\, d\dot{h}\, d\ddot{h}},$$

$$\text{with } \xi = \sqrt{\frac{\bar{P}_O}{\bar{P}_{Om}}}, \quad \bar{P}_{Om} = 16\,\text{dBm}. \tag{51}$$

The forecast of the model matches the measurements very well. This is quite impressive, considering that a simplified and linearized model was used for analysis. The ACLR leaves slightly the range admitted by the W-CDMA standard. This effect can have two different causes: either the DC–DC converter is not capable to follow the envelope of the RF input signal all the time. Or the gain and phase shift of the PA changes with its supply voltage. Such behavior, which was shown for the RMPA2265, makes it not very suitable for an EF PA at all. To emphasize this assumption the ACLR estimation method, presented in [12], is applied on a RMPA2265 whose supply voltage is modulated ideally. The results are also depicted in Fig. 10. They show that even an ideal modulation of the supply voltage would cause a significant rise of the ACLR. Due to the dependency of the PA gain and phase on its supply voltage, the output ripple of the buck converter is mixed with the RF signal. This effect causes the high values of the ACLR (especially at low output powers) in the second adjacent channels. The following properties of the design were observed with an oscilloscope and are completely satisfying.

[2]The test signal has the same setup as the W-CDMA signal used to determine the statistical properties of the envelope.

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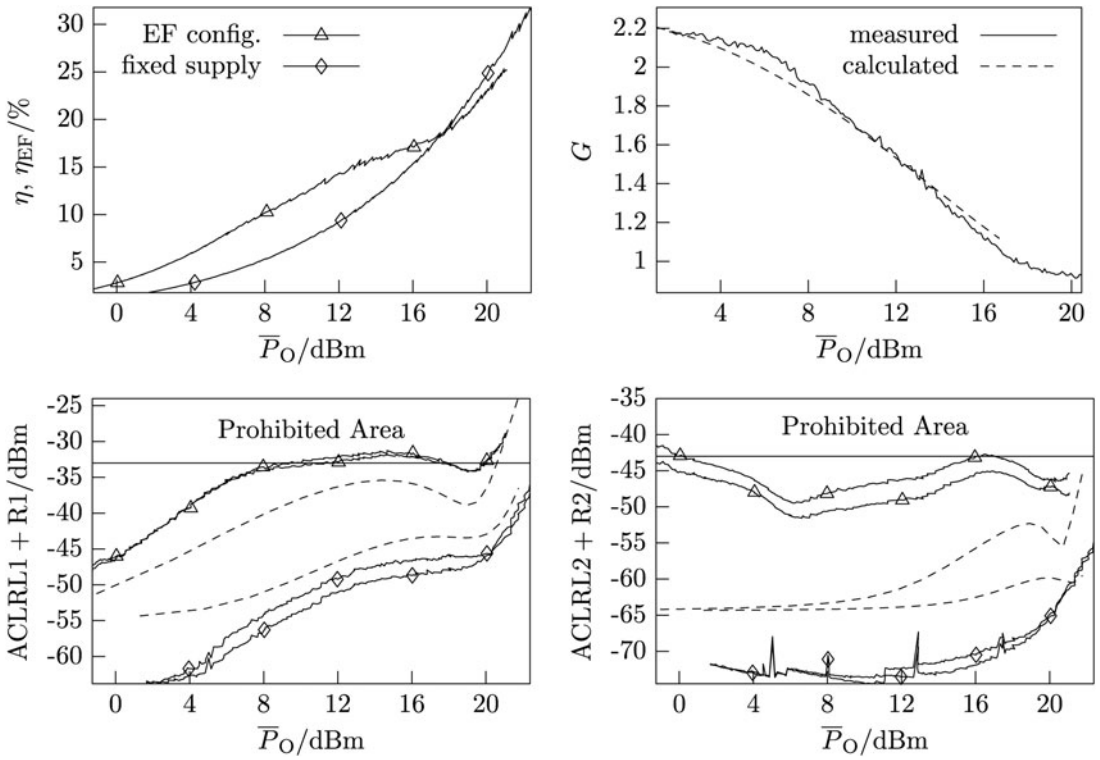

Fig. 10. Comparison between the fixed supply voltage and the *EF* (with the proposed buck converter and an ideal supply voltage modulator) configuration of the RMPA 2265.

The average efficiency gain

$$\bar{G} = \int p_S\left(\bar{P}_O \frac{P_{27dBm}}{P_{16dBm}}\right) G(\bar{P}_O)\, d\bar{P}_O = 2.03 \qquad (52)$$

is obtained by weighting the measured values with their probability. Furthermore, the average efficiency gain with an ideal supply voltage modulator is defined as follows:

$$\bar{G}_I = \int \frac{V_{DD}}{V_E(\xi h)} p_M(h, \dot{h}, \ddot{h})\, dh\, d\dot{h}\, d\ddot{h} = 3.19. \qquad (53)$$

The ratio between these two quantities is approximately the efficiency of the buck converter

$$\frac{\bar{G}}{\bar{G}_I} \approx \eta_B = 63.8\%. \qquad (54)$$

The value of η_B as also derived from the results of the measurements and is very similar to the one which was determined during the parameter optimization (shown in Fig. 6 with a cross).

V CONCLUSION

The buck converter presented in this work, fulfills all requirements of an envelope amplifier for a modern efficiency enhancement system. It shows both a high average efficiency of 63.5% and the dynamic properties to follow the fast changing envelope signal of a W-CMDA modulated RF signal. Because the design only uses CMOS devices, it is perfectly suited for economic large-scale productions. By means of the proposed design flow the circuit can be adapted to a wide range of different communication standards and IC technologies. The base of this flow is the mathematical model of the DC–DC converter and the envelope signal. Its accuracy is confirmed by measurements. In an *EF* configuration the buck converter doubles the average efficiency of an industry standard W-CDMA PA (RMPA2265). The DC current of this PA varies over the wide range from 30 to 160 mA proportional to the square root of its output power. Hence, the RMPA2265 has already – without any efficiency enhancement techniques – a much better back-off efficiency as comparable PAs in class A configuration. That is why the presented design has to cope with a challenge, which cannot be found for a setup with a class A PA. A high average efficiency of the DC–DC converter despite a wide range of its output current.

Due to restrictions of the used technology only small supply voltages could be used. The employment of technologies which are better suited for switching regulators could increase the supply voltage and also the efficiency gain significantly.

ACKNOWLEDGEMENTS

This work was partly funded by the Federal Ministry of Education and Research (BMBF) in the excellence cluster Cool Silicon, project Cool Broadcast Repeater.

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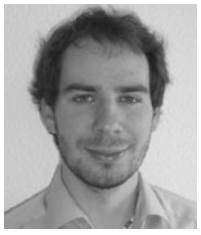

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