An ultra-wideband current-reused LNA MMIC with negative feedback and adaptive bias networks

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Abstract

An ultra-wideband current-reused low-noise amplifier (LNA) monolithic microwave integrated circuit design is presented in this letter. Negative feedback networks are employed at both stages of the proposed LNA to expand bandwidth. Furthermore, source adaptive bias networks is designed in the first stage and combined with a current-reused construction to acquire a compact chip size and maintain low power consumption. Then, the validation of design theory is implemented by employing a 0.15-μm gallium arsenide pseudomorphic high-electron-mobility transistor process. The measured results show that the proposed LNA achieves a small signal gain of 15.5–17.8 dB, a noise figure of 3–3.65 dB, and an output 1 dB compression point ($OP_{1\,dB}$) of 14.5–15.5 dBm from the target bandwidth of 2–18 GHz. In addition, the fabricated LNA consumes 220 mW from a 5 V supply and occupies a chip area of 1.2×1.5 mm^2.

Introduction

The development of transmission/reception (T/R) components in wireless communication systems is inseparable from the rise of II—V semiconductors [1, 2]. Low-noise amplifiers (LNAs), as essential component of wireless receiving systems, are vital for improving the signal transmission quality of communication systems [1–5]. As a result, driven by application requirements, achieving bandwidth expansion and a more compact chip size of the LNA monolithic microwave integrated circuit (MMIC), as well as reducing power loss, has become the most promising research topic at present [1–5].

In recent years, various technologies have been proposed to promote the performance of LNA MMIC, such as current-reused construction [1, 2, 6–13] negative feedback networks (NFNs) [3, 4, 7, 14], and reconfigurable techniques [15]. Specifically, as shown in reference [14], an LNA MMIC operating at 0.1–20 GHz is presented by using feedback techniques, achieving a noise figure (NF) of 3.1–5.8 dB, an output 1 dB compression point ($OP_{1\,dB}$) of 7.8–12.7 dBm, and a power consumption of 505 mW. In reference [15], based on reconfigurable technology, an LNA MMIC working at 12–20 GHz is presented, occupying a chip area of 2×1.8 mm^2, achieving an $OP_{1\,dB}$ of 2.2–5 dBm, and a power consumption of 227.5 mW. As a result, it can be seen that these reported works demonstrate some technological advantages in promoting certain performance of LNA. However, as is well known, many technical indicators of LNA, such as operating bandwidth, $OP_{1\,dB}$, power loss, NF and chip area, have a trade-off pattern, meaning that in practical engineering applications, these technical indicators need to be at an acceptable level, which is extremely important for the engineering design of LNA.

In this letter, an ultra-wideband (UWB) LNA MMIC operating in the S-C-X-Ku band is presented by employing current-reuse construction. Meanwhile, an NFN and source adaptive bias circuit are used to achieve bandwidth expansion and the compact chip size of the proposed LAN MMIC. Subsequently, theoretical verification is carried out based on a 0.15-μm gallium arsenide (GaAs) pseudomorphic high-electron-mobility transistor (pHEMT) process. The measured results demonstrate the effectiveness of the proposed design method.

UWB LNA MMIC circuit topology and design

The proposed UWB LNA MMIC design is implemented using the 0.15 μm GaAs pHEMT technology of Sanan Semiconductor. In order to balance the size, power consumption, and gain of the chip, a current-reuse topology is adopted, where the two transistors M_1 and M_2 have the
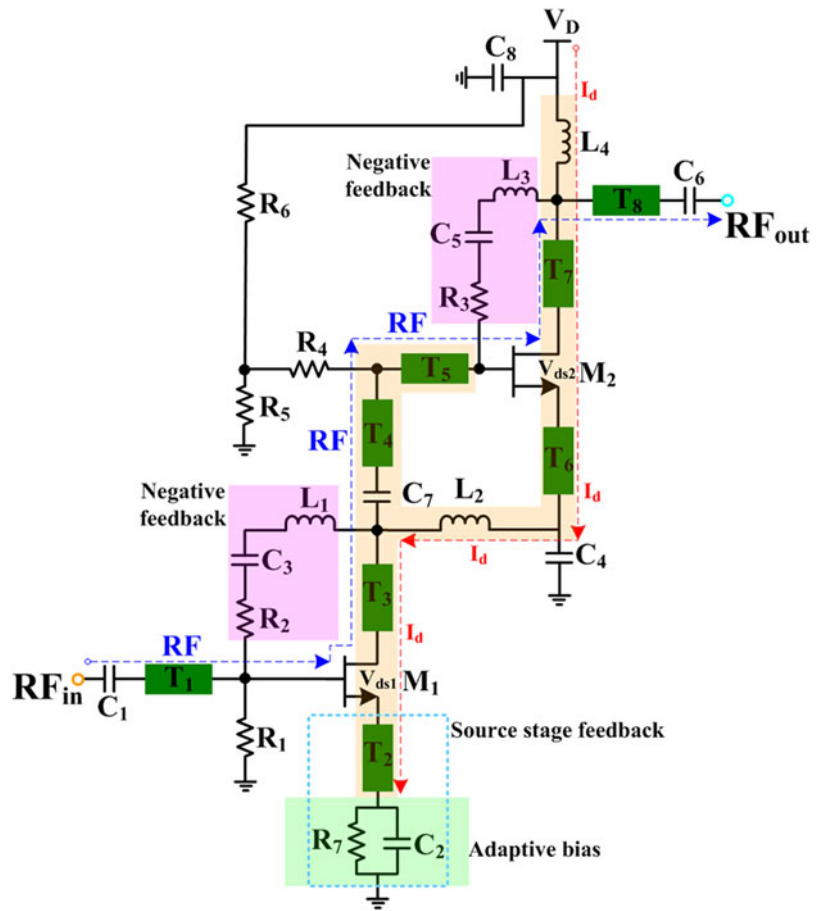
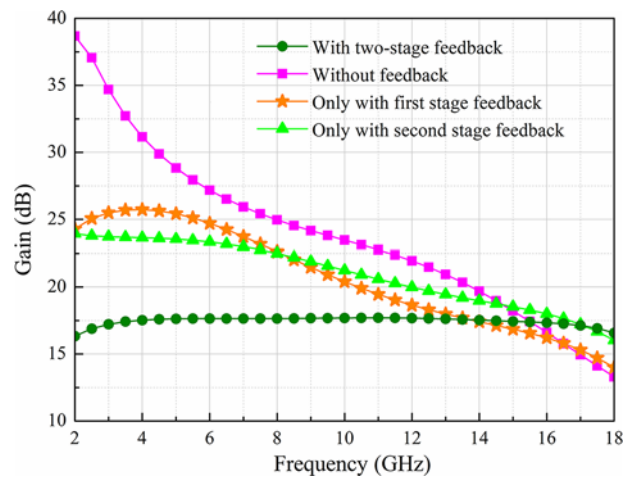**Figure 1.** Circuit schematic of the proposed UWB LNA MMIC.

Table 1. Parameters of the proposed UWBLNA MMIC (UNIT: L, nH; R, Ohm; C, pF; TRANSMISSION LINE-W/L, $\mu m/\mu m$; M, μm^2)

Para	C_1	C_2	C_3	C_4	C_5	C_6
Value	8.7	45.7	1.85	10.23	3.3	1.58
Para	C_7	C_8	T_1	T_2	T_3	T_4
Value	8.7	95	7/620	33/50	25/400	24/620
Para	T_5	T_6	T_7	T_8	L_1	L_2
Value	24/850	33/90	13/485	16/900	1.14	5.4
Para	L_3	L_4	R_1	R_2	R_3	R_4
Value	1.02	5.4	3500	198	193	5000
Para	R_5	R_6	R_7	M_1	M_2	
Value	6000	8000	10	4 × 45	4 × 45	

Para: Parameter.

Figure 2. Simulated gain curves with and without NFNs for the proposed LNA MMIC.

same size, which is 4 × 45 μm. Based on this, the proposed LNA schematic is presented in Fig. 1, which includes two NFNs, a source adaptive bias circuit, and a current-reuse construction. All parameter values in the circuit are given as shown in Table 1.

As demonstrated in Fig. 1, the transmission path guided by the red dashed line with the drain current I_d is the direct-current (dc) path of the proposed LNA. The circuit located in the orange shaded area is the current-reuse construction used, where transistors M_1 and M_2 share the same drain supply, which can effectively reduce the power loss of LNA MMIC. The transmission path guided by

the blue dotted line with the radio frequency (RF) mark is the RF path of the proposed LNA, in which the inductor L_2 is used to prevent the RF signal from leaking into the dc path, and similarly, the capacitor C_7 is used to prevent the dc signal from entering the RF path.

The gate bias voltage (−0.5 V) of the first stage is generated by the drain current of transistor M_2 acting on the resistor R_7 in the adaptive bias network, which can eliminate the design of the
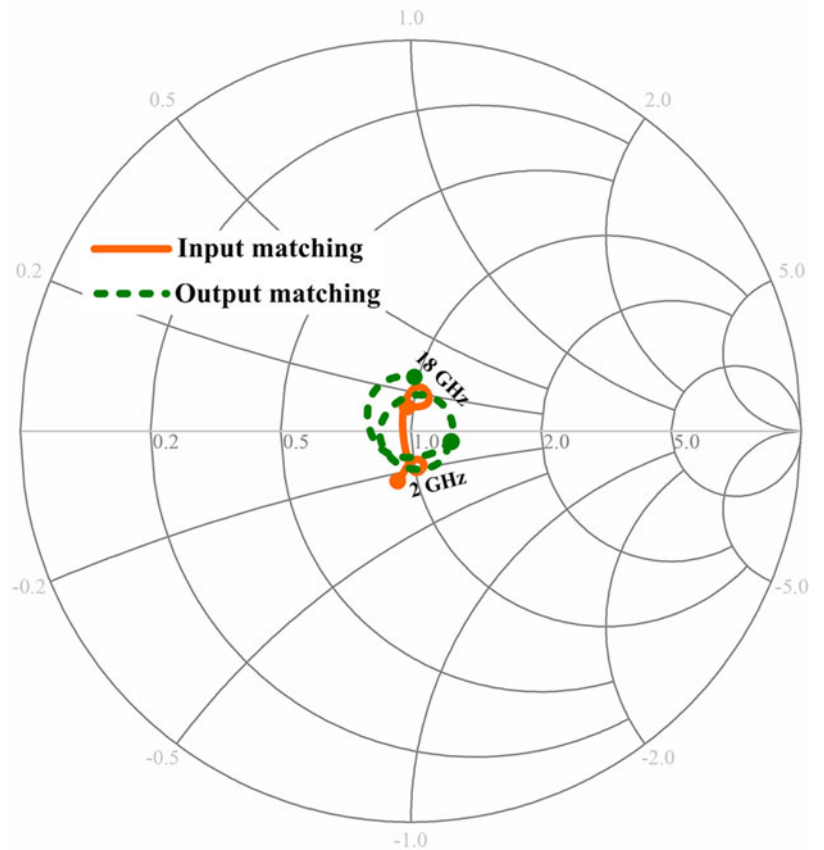
Figure 3. The simulated impedance trajectory variation of the input and output of the proposed LNA MMIC in 2–18 GHz.
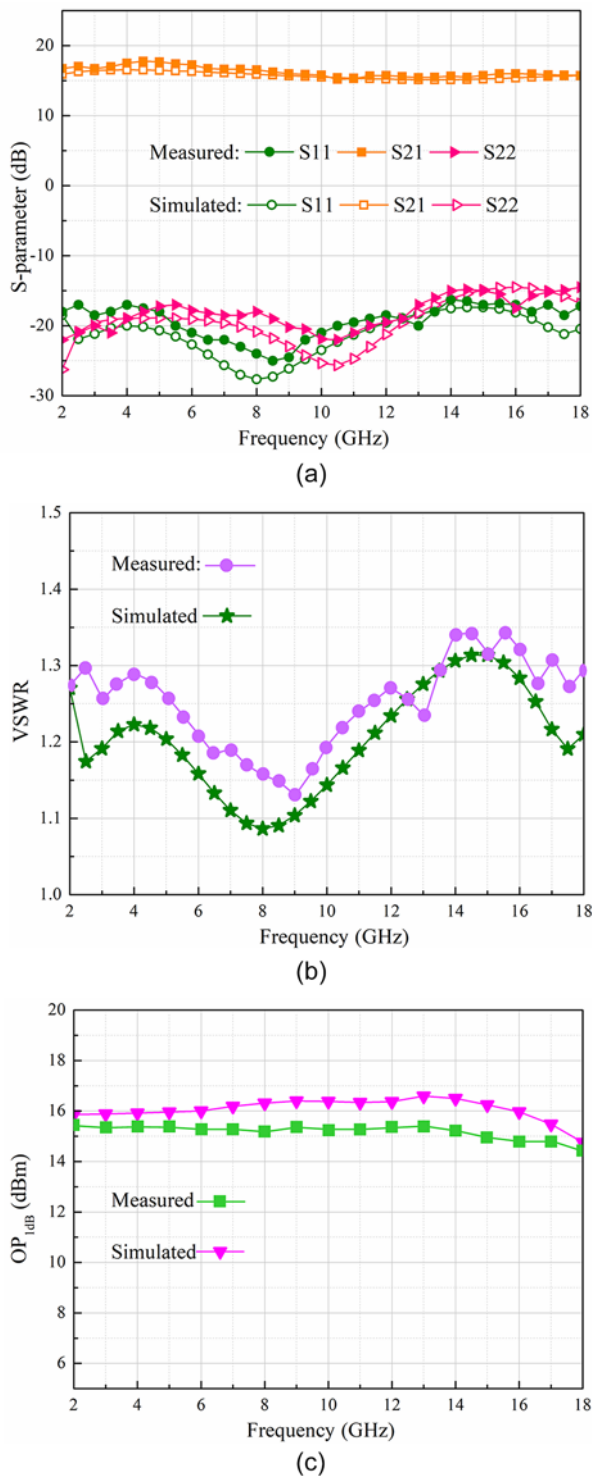
gate bias network of transistor M_1, weaken the design complexity of the dc power supply network, and help reduce the overall size of the chip. In addition, the adaptive bias network RC located at the source of transistor M_1 combined with microstrip line T_2 can form source stage feedback to achieve bandwidth expansion, specifically manifested in the capacitive reactance decreases with increasing frequency, which helps to compensate for the inherent gain roll-off of the transistor [16]. The gate bias voltage of the second stage transistor M_2 is provided by a resistive voltage divider network composed of R_5 and R_6, which also helps to reduce the design complexity of the dc power supply network. In addition, the resistor voltage divider network composed of R_5 and R_6 is also used to promote the $OP_{1\,dB}$ of LNA, which is mainly achieved by manipulating the drain source voltage (V_{ds1} and V_{ds2}) distribution of transistors M_1 and M_2 using the ratio of R_5 and R_6. For this design, the $OP_{1\,dB}$ of LNA is determined by the second stage transistor M_2, while for the current-reused structure, the drain current (I_{ds}) of the two stage transistors is the same. Therefore, increasing the output power of the second stage can be achieved by increasing the drain source voltage V_{ds2} of M_2.

Moreover, in order to compensate for the inherent gain roll-off characteristics of transistors, feedback techniques are also introduced into the proposed LNA MMIC circuit design. As a result, a NFN composed of R-L-C is employed in the two stages of the proposed LNA to achieve bandwidth expansion, as exhibited in Fig. 1. Figure 2 demonstrates the simulated gain curves with and without NFNs for the proposed LNA MMIC, where C_3 and C_5 are used to isolate dc from the gate and drain stages of transistors M_1 and M_2. As displayed in the simulation results in Fig. 2, it can be seen that the LNA MMIC without the addition of NFN exhibits a more obvious gain roll-off characteristic. Compared to introducing feedback
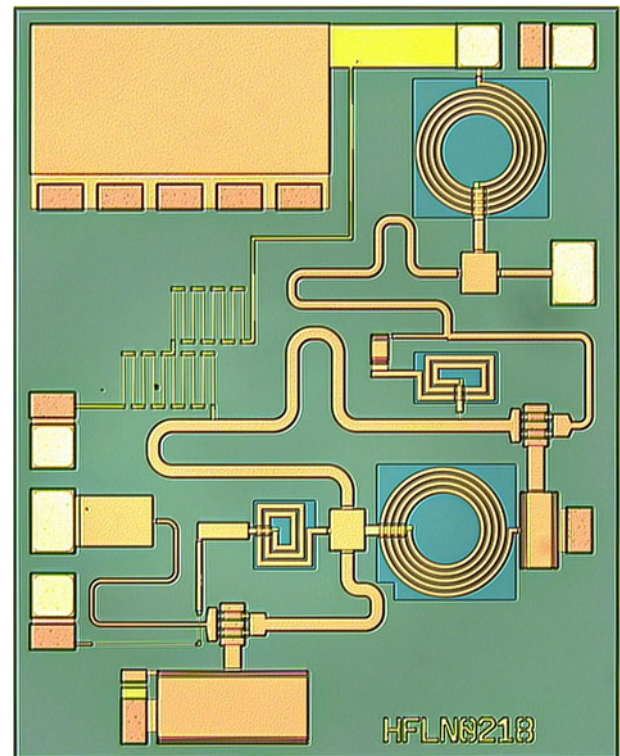
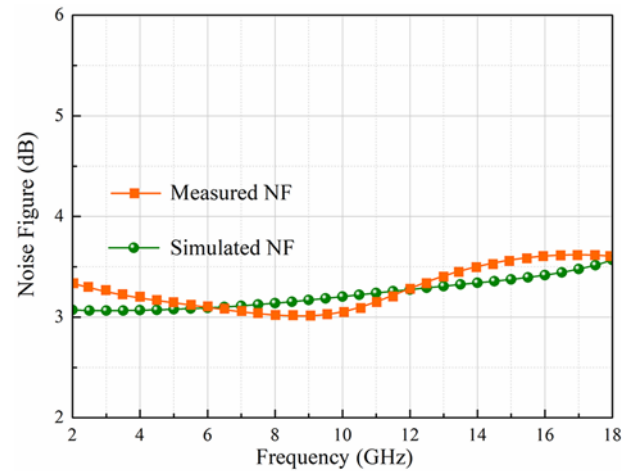**Figure 4.** Chip microphotograph of the proposed UWB LNA.

circuit only in the first or second stage, the bandwidth expansion effect generated by introducing R-L-C NFN in both stages of
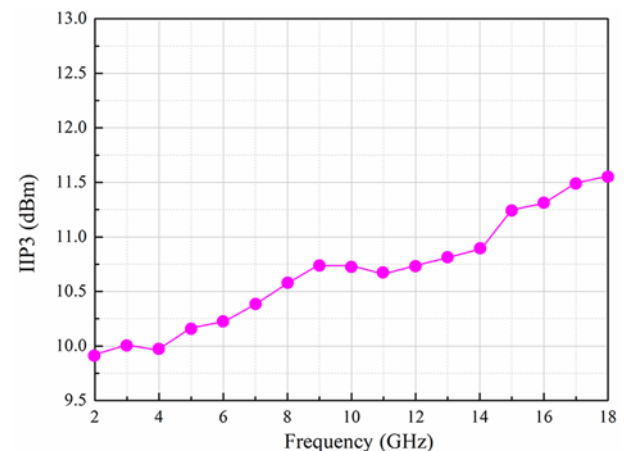
Figure 6. Measured result of NF from 2–18 GHz.

Figure 7. Measured IIP3 of the designed amplifier against frequency.

Figure 5. Simulated and measured results of small-signal. (a) S-parameter. (b) VSWR. (c) OP$_{1\,dB}$.

terminals of the proposed LNA MMIC are plotted in Fig. 3, where the orange solid line represents the input terminal and the green dashed line represents the output terminal. As exhibited in the figure, the impedance completed at both the input and output terminals varies closely around the 50Ω at the center of the Smith chart, indicating the rationality of the matching network design.

Simulated and measured results

As a validation of the proposed design method, a prototype is designed, fabricated, and measured using a 0.15-μm GaAs pHEMT process. Figure 4 demonstrates a photograph of the proposed UWB LNA MMIC with a chip area of 1.2 × 1.5 mm². The measured LNA consumes a 44-mA dc current from a 5-V dc supply, which generates a 220-mW dc consumption.

Subsequently, the small signal measurement is executed, and the measured results for the S-parameter are plotted in Fig. 5(a). As displayed in the figure, it can be seen that within the target frequency band of 2–18 GHz, the proposed LNA MMIC achieves S$_{21}$ between 15.5 and 17.8 dB, while S$_{11}$ and S$_{22}$ are maintained below −16.3 and −14.5 dB, respectively. Furthermore, the voltage-standing-wave ratio (VSWR) at the input of the measured LNA

amplification topology is more obvious through compensating for the gain roll-off of the transistor.

To verify the conversion performance of the input impedance and output impedance to 50Ω completed by the input matching network of the first stage and the output matching network of the second stage of the topology network presented in Fig. 1, the simulated impedance trajectories of the input and output

Table 2. Comparisons with state-of-the-art integrated LNA MMIC

Ref	BW (GHz/%)	Gain(dB)	S_{11}(dB)/S_{22}(dB)	NF(dB)	OP_{1dB} (dBm)	Area (mm^2)	P_{DC} (mW)	FOM	Process
[10]	17−28 (49)	14−17	<−3#, <−10#	2.2−4#	6	1.5	30.03	6.8	0.15 μm/GaAs
[14]	0.1−20 (198)	27.4−29.8	<−10, <−10	3.1−5.8	7.8−12.7	1.53	505	24.5	0.15 μm/GaAs
[15]	12−20 (50)	20.1−28	<−10, <−10	1.23−1.51	2.2−5	3.6	227.5	11.7	0.15 μm/GaAs
[17]	33−38 (14.1)	26	<−7, <−10	2	20	5.5	564	24.6	0.1 μm//GaN
[18]	3.1−10.6 (110)	11.1#	<−11, NA	4.5−5.8	NA	0.46	9	NA	0.18/CMOS
[19]	2−42 (182)	11.1−14.1	<−5, <−5	2.1−4.4	14.7	1.53	129	16.67	0.15 μm/GaAs
[20]	18−56 (103)	16−21.5	<−5, <−5	2.2−4.4	10−20	4.8	1400	3.66	0.1 μm/GaN
[11]	3.2−14.7 (127)	34	NA	1.3−1.6	NA	3.75	45	NA	0.15 μm/GaAs
[12]	3.8−19.8 (135)	18.5−21.5	NA	1.1−3	NA	1.5	40	NA	0.1 μm/GaAs
[13]	2.5−31 (170)	33.5	NA	1.6	NA	3.75	60	NA	0.15 μm/GaAs
This work	2−18 (160)	15.5−17.8	<−16.3, <−14.5	3−3.65	14.5−15.5	1.8	220	19.3	0.15 μm/GaAs

#Estimated value from the figure.

MMIC is presented in Fig. 5(b). As exhibited in the figure, the implemented VSWR is between 1.127 and 1.35 in the entire S-C-X-Ku-band. Meanwhile, Fig. 5(c) demonstrates that the measured $OP_{1\,dB}$ is 15 ± 0.5 dBm for $V_D = 5$ V over the 2–18 GHz.

The NF measurement of the fabricated LNA MMIC is performed, and the simulated and tested results are exhibited in Fig. 6, where the measured NF is between 3 and 3.65 dB from 2 to 18 GHz. It should be noted that the lack of outstanding NF performance of the proposed LNA is mainly attributed to two aspects. First, in the target frequency band of 2–18 GHz, in order to balance the NF performance in the high-frequency band, it is necessary to sacrifice the noise performance in the low-frequency band to ensure that the NF of the entire design frequency band is at an acceptable level. The second is that $1/f$ noise within the entire design frequency band can also have a significant impact on the NF of LNA.

Besides, the measured the input third-order intercept point (IIP3) of LNA in the target frequency band range of 2–18 GHz using a two-tone signal with an interval of 1 MHz and an input power of 5 dBm, is shown in the Fig. 7. It can be seen that within the target frequency band, the proposed LNA MMIC achieves IIP3 between 9.8 and 11.6 dBm.

Based on reference [21], a modified figure of merit (FOM) considering the center frequency, bandwidth, gain, NF, dc power, and $OP_{1\,dB}$, is adopted to conduct a state-of-the-art comparison as follows [21]:

$$FOM = 20 \log_{10} \left(\frac{Gain\,[abs] \cdot OP_{1dB}\,[mW]}{(NF_{\min}\,[abs] - 1) \cdot P_{dc}\,[mW]} \cdot \frac{BW\,[GHz]}{f_0\,[GHz]} \right) \tag{1}$$

where f_0 is the center frequency. As a result, a comparison between the proposed LNA MMIC and other published LNA MMICs is presented in Table 2. By comparing the performance parameters in the table, it can be concluded that the implemented LNA demonstrates a comprehensive technical advantage.

Conclusion

An UWB current-reused LNA MMIC with two-stage cascading is presented in this letter for wireless communication. A NFN and source adaptive bias circuit are introduced to achieve bandwidth expansion and compact chip size for the proposed LAN MMIC. The proposed design scheme has been validated by fabricating the LNA in 0.15-μm GaAs pHEMT technology, which occupies a chip area of 1.2×1.5 mm^2. The measured results manifest that the proposed LNA achieves a small signal gain of 15.5–17.8 dB, a NF of 3–3.65 dB, and an $OP_{1\,dB}$ of 14.5–15.5 dBm from the target bandwidth of 2–18 GHz, indicating potential commercial value in wireless communication.

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Competing interest. The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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